PDN OPTIMIZATION OF 3DIC'S USING TSV TECHNOLOGY

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Abstract: Through Silicon-via [TSV] and die-stacking are the two important technologies available for three-dimensional Integrated Circuits [3D IC's]. This TSV technology brings the performance improvement through the reduction of wire length and footprint area. But compared to 2-D IC's, the 3-D IC's have several challenges for power delivery network design due to larger supply currents and longer power delivery paths. In 3-D IC, the power delivery network with flip chip package is mainly compared of Power/Ground [P/G] bumps and P/G TSV's. It is very important to optimize their P/G bumps and P/G TSV's together by satisfying the IR-drop constraints because the number of P/G bumps is limited and the size of P/G TSV is larger than that of standard cell. In this paper, we obtained an effect of the number of power bumps and power TSV's on the IR-drop in 3-D IC floor plan level and proposed the methodology, which will optimizes the number and position of both power bumps and power TSV's at a time.

Keywords: 3D IC's, TSV, P/G bumps, PDN.

I. INTRODUCTION:

3D-IC appears to be a cost effective approach to manage increasing memory needs and shrinking share of logic area. This 3D-IC [9] also offers an attractive solution for overcoming the barriers to interconnect scaling, thereby offering an opportunity to continue performance improvements using CMOS technology, with smaller form factor, higher integration density, and the support for the realization of mixed technology chips. Among several 3D integration technologies [3], TSV (Through-Silicon-Via) approach is the most promising one and therefore is the focus of the majority of 3D integration R&D activities [10]. A TSV-based 3D chip consists of multiple device layers stacked together with direct vertical interconnects (through-silicon vias, or TSVs) tunneling through them. 3D-IC along with through silicon-via (TSV) has been introduced mainly to overcome the disadvantages of transistor size scaling. TSV is a high performance technique to create 3D packages and 3D-IC, compared to alternative such as package-on-packages, because the density of the via is substantially higher. 3D-IC using TSV's improve performance by reducing wire length, interconnect delays and foot area of chip as compared to 2D IC's. Even though manufacture/process techniques for 3D integrations are nearly mature [10], [11], and 3D ICs offer tremendous benefits, one of the challenges that hinder the successful adoption of 3D technology is the lack of commercially available electronic design automation (EDA) tools and design methodologies for 3D-IC [12]. The absence of EDA tools that can explore the design space is an impediment to researchers and industry practitioners in their quest for the adoption of this new technology. Consequently, there are many R&D activities on developing EDA tools and methodologies tailored specifically for 3D-IC designs. 3D IC design is fundamentally related to the topological arrangement of logic blocks. Therefore, physical design tools for 3D circuits are important for the adoption of 3D technology [13]–[16]. Among various physical design problems, floor planning and power/ground (P/G) network synthesis both play an important role in the early stages of the IC design flow:

i. The floor planning stage defines the placement of the major blocks and components of the IC, affecting the optimization results of the subsequent stages including placement and routing.

ii. P/G network synthesis sizes and places the power and ground lines for the chip. There are two important optimization goals for P/G network synthesis: (1) Minimize IR drop, which can have negative impact on the performance of the circuit. IR drop has become more important as technology scales, because as the wires shrink with smaller feature sizes, the resistances along the power lines increase. (2) Minimize the routing area of the P/G wires, which causes congestion during later routing stages. However, there is potential conflict between these two optimization goals. For example, using wider wires for P/G network could help reduce IR drop but the routing area is increased. Consequently, a design tradeoff between the P/G area and IR drop is needed. Even though there exist studies on 3D IC floor planning, most do not consider the P/G delivery to the blocks. On the other hand, there has been little research on 3D P/G networks. To help explore the 3D design space and help fill the need for 3D EDA tools.

iii. Satisfying the IR drop constraint becomes challenging because the resistance of P/G wire is increased due to shrinking wire and increasing the power consumption of chip as technology advances. IR-drop problems are still challengeable in 3-D ICs. Thus, we proposed the power delivery network model in 3-D ICs which satisfying the IR-drop constraint.

iv. Investigating an effect of P/G bumps and P/G TSVs count on the IR-drop were power is supplied by P/G bumps and delivered to the each die by P/G TSVs. Therefore, the IR-drop is largely affected by P/G bumps and P/G TSVs. We investigated an effect of the number of P/G bumps and P/G TSVs on the IR-drop in the 3D floor plan level.

v. Optimizing the number of P/G bumps is limited and an excessive use of P/G TSVs causes a routing congestion. However, there are no power network models that co-optimize the number and position of P/G bumps and P/G TSVs. The proposed methodology optimizes the number and position of P/G bumps and P/G TSVs.

II. MOTIVATION AND RELATED WORK

In this section, we first discuss the motivation of our work, and the present the related work.

A. Why 3D Floor plan and P/G Network is needed.

In a traditional design flow, floor planning and P/G network design are two sequential steps: the floor planning is performed first to optimize chip area and wire length, and then the P/G network is synthesized. However, it has been shown by Liu and Chang [17] that, in 2D IC design, if the floor plan does not consider the P/G network, the resulting floor plan may lead to an inefficient P/G network with high IR drops and several P/G voltage violations. It is very difficult to repair a P/G network after the post-layout stage, so the P/G network should be considered as early as possible. In Floor plan and P/G co-synthesis, the P/G network is created during floor planning. During co-synthesis, the floor plan not only tries to minimize the wire length and area of the design, but also ensures that there are no power violations to the blocks in the floor plan. This results in a floor plan with an efficient P/G network.

B. Related work:

K. Chen and C.S. Tan proposed [1]; a various Integration schemes and key enabling technologies for wafer-level 3D IC are reviewed & discussed. Stacking orientations [face up or face down], methods of wafer bonding formation TSV [via first, via middle, via last] and singulation level (wafer to wafer of chip to wafer) are options for 3D IC integration schemes. Key enabling technologies, such as alignment, C_U- C_U bonding & TSV fabrication, are described as well. Improved performing, such as lower latency & higher bandwidth, lower power consumption, smaller form factor, lower cost & heterogeneous Integration of disparate functionalities are made possible in the next generation of electronics products with the realization of 3D IC. K. Dae Hyun et al. [2] introduced a Through Silicon via (TSV). This TSV is the enabling Technology for the fine- grained 3D Integration of multiple dies into a single stack. There TSV's occupy non-negligible Silicon area because of their sheer size. This significant Si area occupied by the TSV's and the interconnections made to the TSV's greatly affect area, power, performance & reliability of 3D-IC's layouts. Well-managed TSV's alleviate congestion, reduce wire length and improve performance, whereas excessive TSV's not only increases the die area, but also have negative impact on many design objectives. Yu Zhong, M.D.F.Wong [3], implemented a power grid network in VLSI circuits, which provides adequate input supply to ensure reliable performance. And they also proposed an algorithm to find the placement of power pads that minimize not only the worst voltage drop but also the voltage deviation across the power grid. Algorithm uses simulated annealing to minimize the total cost of voltage drops. The key enables for efficient optimization is a fast localized node-based iterative method to complete the voltage after each movement of pads. And results show that algorithm demonstration good runtime character for power grid with large number of pad candidates in Multi-million-size circuits. P. Falkenstern et al. [4] proposed a Three-dimensional integrated circuits (3-D IC) floor plan and power/ground network co-synthesis, in which 3D IC's are currently being developed to improve existing 3D design by providing smaller chip areas & higher power ad lower power consumption & however, before 3D IC's become a viable technology, the 3D design space needs to be fully explored & 3D EDA tools need to be developed.In this paper, we investigated an effect of the number of P/G bumps and P/G TSVs on the IR-drop in 3D IC floor plan level and proposed the methodology that reduces the number of P/G bumps while the number of P/G TSVs and maximum IR-drop are comparable to the previous methodology as in [5]. The rest of the paper is organized as follows: Section II presents the related works. Section III presents power delivery network analysis. Section IV describes the proposed methodology presents. Section V simulation results using the 3-D floor plan tool. Finally, a conclusion is given in Section IV.

III. POWER DELIVERY NETWORK ANALYSIS

Power delivery network (PDN) is mainly used for the following reasons:

a. To carry current from pads to transistors on chip.
b. To maintain stable voltage with low noise.
c. To provide average and peak power demands.
d. To provide current return paths for signals.
e. To avoid electro migration and self heating wear out.
f. To consume little chip area, wire and easy to layout.

We analyze the power delivery network by using the circuit model [4-5]. Figure 1(a) shows the power delivery network based on the mesh grid structure.

The power bumps supply the power delivery network with supply voltage and power pins which are connected with modules will consume a given amount of current at the given nodes. In Fig. 1(b), the circuit model regards the power wires as resistances, the power pins as independent

current sources and the power bumps as voltage sources

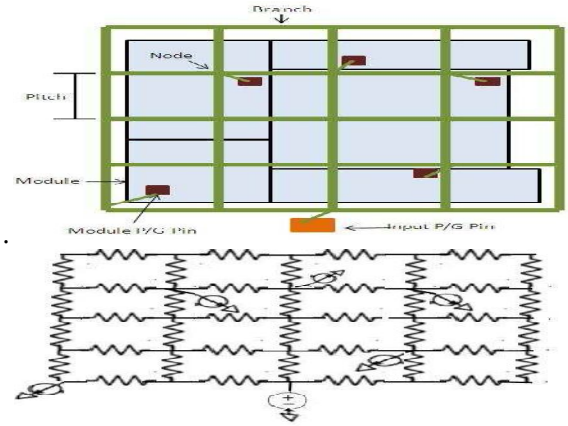

Figure 1. Power delivery network in 2-D IC. (a) Power delivery network based on the mesh grid structure, (b) circuit model of power delivery network.

Figure 2 shows the circuit model of a 3D power delivery network. We assume that adjacent dies are bonded with face to- back (F2B) [5]. While power TSVs are routed through local vias in each die, power bumps are placed on the bottom-most die among the C4 bumps. In this model, the power supplied to the bottom-most die through the power bumps is delivered to the upper die through the power TSVs. Then, modified nodal analysis (MNA) equation is widely used to estimate the IR Figure drop [6]. In this analysis, we focus on a steady-state case (DC analysis) and ignore effects of on-chip inductance when estimating the IR-drop since the on-chip inductance in the power delivery network is too small to affect the results of our analysis [5].

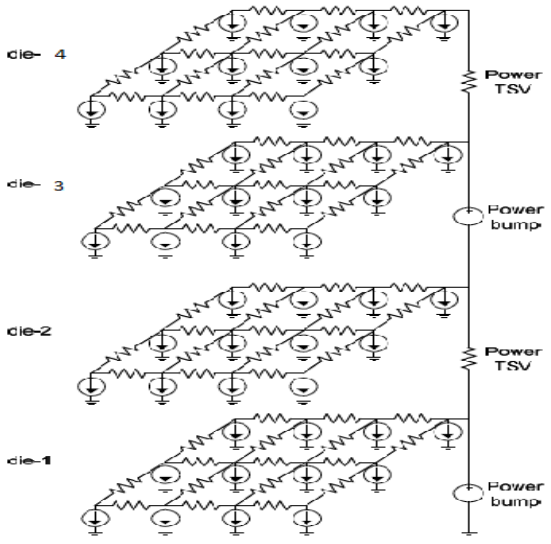

Figure2. Circuit model of 3-D power delivery network.

IV. PROPOSED METHODOLOGY

The proposed co-optimization methodology for power bump and power TSV placement is shown in Fig. 3. The proposed methodology is composed of three steps. The first step is constructing the initial power delivery network step, the second step is finding the initial position of power bump step and the third step is satisfying the IR-drop constraint step. First step: the initial power delivery network is constructed in this step. We assume that each die is the same size, the power ring is routed around a core and power stripes are routed in a mesh grid structure with predetermined pitch. The power TSVs are placed on the power core ring in the same pitch as the power stripes because those power TSVs do not affect the routing resource inside the core region [7]. Second step: to find the initial position of power bump, we place the P/G bumps on all candidate nodes. After placing the power bumps on all candidate nodes, we update the circuit and estimate the IR-drop. After estimating the IR-drop, we can find the worst IR-drop node in the bottom-most die. The lowest voltage node is defined as the worst IR-drop node and it determines the position of the first power bump at this time. Finally, all the power bumps are removed except the power bump on the worst IR-drop node. Figure 4 shows the second step of the proposed methodology.

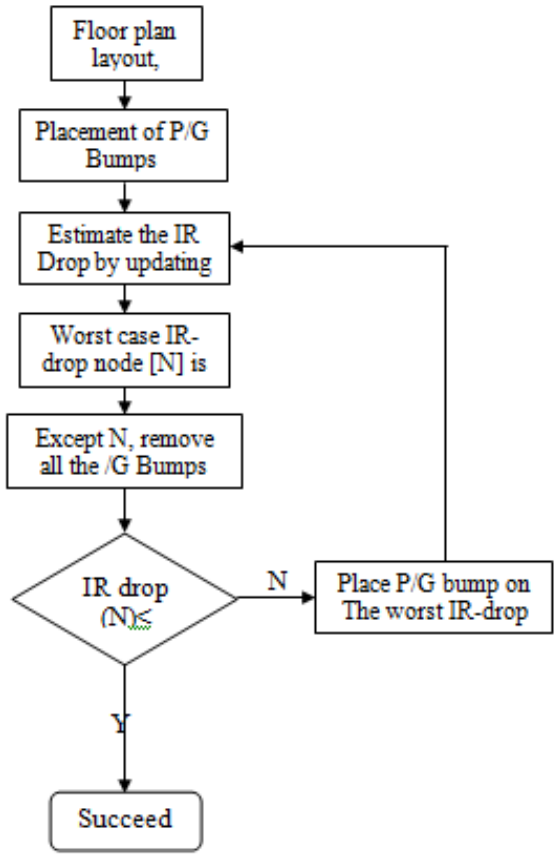

Figure 3. Flow chart of the proposed methodology. node determines the position of first power bump, (b) all the power bumps are removed except the power bump on the worst IR-drop node.

In Fig. 4(a), the power bumps are placed on all candidate nodes in bottom-most die and we can find the worst IR-drop node which determines the position of the first power bump in Fig. 4(b).

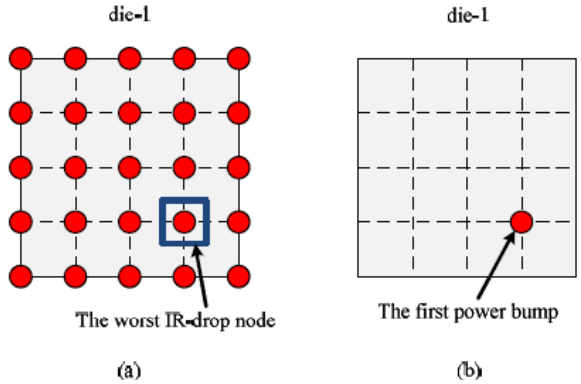

Figure 4. The second step of proposed methodology. (a) the power bumps are placed on all candidate nodes in bottom-most die and the worst IR-drop

Third step: to satisfy the IR-drop constraint, we re-estimate the IR-drop in all dies and again find the worst IR-drop node. Because the power TSVs is already placed on the power core ring as describe above, power is delivered to all dies and we can estimate the IR-drop in all dies. Then, the third step is divided into two cases: the worst IR-drop node is in the bottom-most die and the worst IR-drop node is not in the bottom-most die. If the worst IR-drop node is in the bottommost die, we only place the power bump on the worst IR-drop node as shown in Fig. 5(a). If the worst IR-drop node is not in the bottom-most die, we place both power bump and power TSV on the worst IR-drop node as shown in Fig. 5(b). The power TSV is placed from the current die to the bottom-most die straightly. The third step is repeated until all nodes satisfy the IR-drop constraint. By using the proposed methodology, we can reduce the number of power bumps while the number of power TSVs and maximum IR-drop are comparable to the previous methodology as in [5].

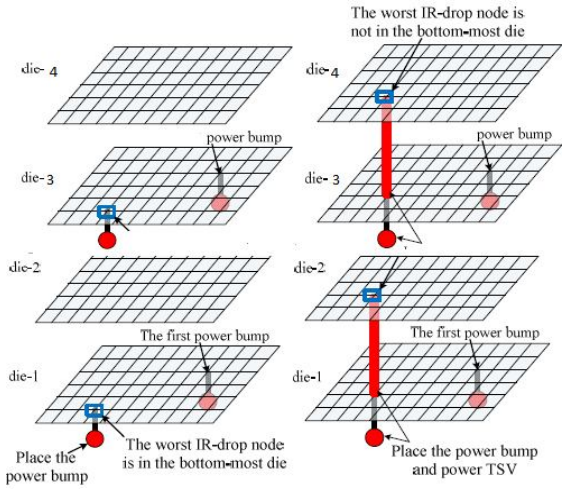

Figure 5. The third step of proposed methodology. (a) the case one: the worst IR-drop node is in the bottom-most die, (b) the case two: the worst IR drop node is not in the bottom-most

V. SIMULATION RESULTS

Our simulations were implemented on HSPICE. We assumed four die-stacked 3-D ICs and modified the 3DFP open source tool that as in [4] and Parquet as in [8] to obtain floor plan results. As in [4-5], we set the input voltage at 2.0 V, the resistance of a power bump at 20 mΩ, the resistance of a power TSV at 10 mΩ and the sheet resistance of the metal layer at 5 mΩ. The structure of the power delivery network was an NxN uniform mesh grid structure with the pitch of power stripes at 5 μm. The simulations include an effect of the number of power bumps and power TSVs on the IR-drop as well as the proposed power bump and power TSV placement methodology. Table I and Table II represents the effect of power bumps, power TSV's on IR drop respectively. Table III shows the area, power, mesh count and number of candidate nodes of MCNC benchmark circuits

Table-I Effect of the number of power bumps on the IR-drop.

No of Power Bumps	Worst Voltage [V]
5	0
10	0.2
15	0.4
20	0.65
25	0.72
30	0.85
35	0.88
40	0.92

Table-II Effect of the number of power TSVs on the IR-drop..

Circuit	Non –regular P/G TSVs [5]			Ours		
	# of power bumps	*# of power TSVs*	*Maximum IR-drop (mV)*	*# of power bumps*	*# of power TSVs*	*Maximum IR-drop (mV)*
Ami33	200	84	45.2	12	52	46.4
Hp	600	180	47.6	30	160	47.8
Ami49	600	250	50.4	65	210	50.6
Xerox	600	186	48.3	54	192	48.3

Table III. Comparison of results by non-regular power tsvs and proposed algorithm

No of Power Bumps	Worst Voltage [V]
100	0.42
120	0.53
140	0.65
160	0.73
180	0.84
200	0.92

CONCLUSION

In this paper, the methodology for optimizing the number and position of both power bumps and power TSVs is proposed and the effect of the number of power bumps and power TSVs on the IR-drop in a 3-D IC floor plan level was also obtained. By considering the IR-drop and reducing the number of power bumps, a more efficiently designed power delivery network can be synthesized, which can improve the performance of chip design. And the simulation results show that the proposed methodology is effective in optimizing the power bumps and power TSVs for power delivery network in 3-D ICs.

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