DESIGN OF LOW POWER 4-BIT BCD ADDER USING REVERSIBLE GATES

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Abstract- Reversible logic is emerging as an important research area having its application in diverse fields such as low power CMOS design, digital signal processing, cryptography, quantum computing and optical information processing. The proposed BCD adder is efficient in terms of power dissipation. Various technologies are going to be used and respective power dissipation will be compared. Logic Gates such as AND, OR, NAND (Except NOT) gates are not reversible that is inputs cannot be recovered from the output. On the other hand, in Reversible Logic Gates inputs can be recovered completely from the output that is there is one to one mapping between inputs and outputs. Reversible logic gates use less power compared to classical gates and under ideal condition.

Keywords- HNG, NG, RPS gate, BCD Adder.

I. INTRODUCTION

Reversible gates perform a logic computation without a loss of information. A reversible conventional BCD adder was implemented using HNG gates. In this project we implemented BCD Adder using RPS gates. This effects an improved reversible decimal adder with reduced logical complexity and number of garbage outputs.

In this project the design of 4-bit BCD adder using reversible gates is done

II. IMPLEMENTATION

The implementation of BCD adder using RPS. In this totally 9 RPS gates with garbage outputs.

The circuit generates a correction bit ‘L’ or Decimal C\text{OUT}L=C\text{OUT}+S_3(S_1+S_2)

And total sum delay T_{\text{sum-digit}}

T_{\text{sum/conventional}}=N T_{\text{dcout}}+T_{\text{sum-digit}}

For 4 digit BCD adder the delay is 36 and N-digit BCD adder the delay is 9N.

Proposed BCD adder
Design of Low Power 4-Bit BCD Adder Using Reversible Gates

RESULT TABLE

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Technology</th>
<th>(V_{dd}) (V)</th>
<th>No. of Metals</th>
<th>Power Dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BCD Adder</td>
</tr>
<tr>
<td>1</td>
<td>0.12µm</td>
<td>1.2</td>
<td>6</td>
<td>11.281 µW</td>
</tr>
<tr>
<td>2</td>
<td>65nm</td>
<td>0.7</td>
<td>6</td>
<td>0.160µW</td>
</tr>
<tr>
<td>3</td>
<td>70nm</td>
<td>0.7</td>
<td>6</td>
<td>0.242µW</td>
</tr>
</tbody>
</table>

CONCLUSION

From above result table, a conclusion is made that the conventional BCD adder using 70nm technology is
having low power dissipation when compared with other technologies.

The BCD adder using RPS gates using 70nm technology is also having low power dissipation when compared with other technologies. Thus in this project low power conventional BCD adder and Low Power BCD adder are designed and implemented.

**FUTURE SCOPE**

High end technologies can be used for design and implementation of BCD Adder.

**REFERENCES**


