DYNAMIC THERMAL MANAGEMENT USING THERMAL CONTROL CENTERS ON HIGH PERFORMANCE PROCESSORS

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Abstract: Trends in high performance processors are moving towards large scale integration and steady miniaturization to meet the aggressive performance targets. As the technology scales down circuits are providing extra ordinary integration densities with a drawback of increasing power densities. Dissipated power translates into heat and ultimately increases operating temperature causing reliability threats. In addition to this varying workloads will result in run time thermal hotspots. It is recommended to employ on-die thermal sensors for effective thermal management. In this paper we propose control logic for monitoring thermal sensors to achieve effective run time thermal management.

Keywords- Thermal control center, Sensor, Dynamic thermal management, Temperature

I. INTRODUCTION:

In each generation of processors power density has been increasing due to faster scaling of feature size and frequency compared to operating voltage. Operating temperature has been increasing at an alarm rate because of increasing power densities.

Variations within and across workloads lead to run time thermal hot spots. These hot spots will adversely affect leakage, detoriate timing, reducing mean time between failures. Effective assessment and analysis of thermal behavior is crucial to overcome these hotspots. This can be accomplished by using on chip thermal sensors. These sensors should be placed near to hotspots.

Analog thermal sensors can produce voltage or current equivalent to temperature prevailing exploiting the fact that many electrical parameters of semiconductor devices are sensitive to temperature variation. Examples of these parameters include PN-junction forward voltage, threshold voltage, leakage current, and gain [Blackburn 2004].

Thermal diodes should be placed near to hotspots, where as current source and other elements required in data conversion are also sensitive to temperature variations. In order to avoid other components being influenced by hotspot temperature, it is better to place them at a remote location.

All the sensors are scattered all over the virtual functional partition in a chip like single core, say chiplet. Whereas sensor data processing is centralized per chiplet. This processing unit is called Thermal control center(TCC) as shown in figure 1.2. To reduce wiring overhead, data from sensors should be routed to TCC using serial links.

II. SENSOR GROUPING

As discussed in previous section serial interface is the best choice between sensors and Thermal control center to overcome wiring problems. Wiring can be effectively reduced by groping few sensors as a sensor loop and connecting them in daisy chain fashion such that entire sensor loop will take one set of serial links. Each sensor unit will have shifter logic init in order to support serial transmission. Sensor
loops can be formed by interconnecting shift registers in daisy chain.

![Sensor loop diagram](image)

Digital temperature sensor along with shift register as shown in figure 2.1. is considered as a single sensor module. Above sensor loop consist of four sensor modules interconnected, unique sensor ID should be given to each module. Number of sensor modules per sensor loop can be decided based on the width of the result from sensor modules and density of sensor modules in a chiplet. If each sensor module provides 16bit temperature data packet then the result from a sensor loop can be stored in a single 64 bit result register. Result data can be stored according to the sensor ID assigned to the sensor. Co-ordination between all the sensor modules can be achieved by sharing the same control links and ensure that data on these lines should reach the modules at the same time. When Thermal control center sends temperature sample command then all the modules should sample analog temperature value and convert it into digital format and keep the data ready within specified time. If TCC issues a shift command then data should be serially shifted along the shift registers towards serial data output link present at the bottom sensor module. Sensor grouping technique described in this section is suitable in a case where lot of wiring cannot be added at the hot spot prone regions.

III. THERMAL CONTROL CENTER

One disadvantage with the on chip thermal diodes is that threshold current (i.e., the current of the diode at the maximal allowable temperature) depends on the process parameters. Process variations will have lot of impact on these parameters. In order to achieve uniform result from all the sensors for a known temperature each sensor should undergo calibration procedure during manufacturing process. Digital data corresponding to voltage presented by thermal diodes does not correspond to temperature prevailing directly. Calibration equation for sensors can be obtained by mapping the raw temperature data with the known temperature to which chip is subjected.

Thermal control center will handle all the post processing required for mapping raw results from sensors to standard format. Typically these equations contains nested multiplications and divisions like

\[
((AX/a^n)+B)X/b^m
\]

Where A,B are sensor calibration coefficients obtained during manufacturing characterization process and X is raw data. Method of implementation of this equation in TCC depends on the region where it is to be used. If TCC is monitoring a partition of chip which is very prone to temperature variations abruptly then the time required for the equation computation should be less in order to reduce the time lapsed between successive samples. Hardware multipliers and dividers can be employed in such critical regions. In some regions frequency of temperature changes is low and there will be significant ample of time to notice temperature changes. In this case equation multiplications can be implemented by shift and add multipliers using the time available. Choice of implementation should depend on the frequency of temperature changes.

TCC supports different modes of sampling the sensors like periodic sampling, force type sampling, minimum mode, maximum mode. Core regions handle different types of workloads and needs periodic monitoring. Resolution of periodic sampling should also be flexible according to the workload available. Few parts of chip work under low frequency and temperature varies very slowly then force type sampling is the suitable mode for such regions. Force type sampling is triggered with serial communication writes to mode and control registers present in TCC. Maximum mode is helpful in finding the highest temperature encountered by each sensor. TCC will store highest temperature data presented by sensor throughout the maximum mode window. When TCC is operated in minimum mode least value from each sensor through out the window is stored.

Mere sampling of temperature is not enough for dynamic thermal management.TCC has three programmable threshold levels to indicate temperature intensity. Calibrated temperature value from sensor is compared with each threshold value and indication is asserted when temperature crosses threshold value. The response to each threshold is programmable. It is important to note that in a properly designed and managed high-availability and high performance processor, the chip should never reach a temperature that would require a hardware trip to occur, unless a catastrophic physical failure
has occurred in the system. Trip0, Trip1, Trip2 are the three trip levels.

Trip0 can be used to indicate proactively that chip operating temperature is approaching critical value. This trip will interrupt the operating system or send an attention to service element to take preventive actions.

Trip1 will indicate that temperature is reaching the safe operating limit of silicon technology. Hardware can take evasive measures like reducing operating frequency or voltage or instruction dispatch rate.

Trip 2 will indicate that chip is operating in a hazardous state. The only possible solution for this scenario is to replace the component with new one. This situation can be caused due to multiple reasons such as failure in a heat sink or a fan. In such situations the trip level fatal asserts indicating the on chip infrastructure to switch off the clocks instantly to protect the chip from damage. This is only necessary on systems that do not contain a Service Element to protect the system.

IV. SIMULATION RESULTS

Above figure depicts the force type sampling on thermal sensors using register bit manipulation.

Periodic sampling of thermal sensors by TCC is shown in above figure

Calibration equation for a thermal diode sensor of accuracy +/- 5°C has been implemented and above picture shows calibration for a sensor data.

Above simulation result shows the comparison of calibrated sensor data with three threshold levels to assert the trips.

CONCLUSION:

In this paper we presented a control logic design which plays vital role in dynamic thermal management by indicating intensity of temperature prevailing and triggering respective actions. In addition it also supports different types of sampling techniques suitable for regions with varying frequency of temperature changes. Implemented a sample calibration logic in two different ways by taking cores and low frequency operating regions of chip under scope.

REFERENCES:


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