CONCLUSION DATA D FLIP-FLOP DESIGN USING PASS TRANSISTORS FOR LOW POWER APPLICATION

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Abstract- Power reduction in an IC is a serious concern now days. As the MOS devices are wide spread, there is high need for circuits which consume less power, mainly for portable devices which run on batteries, like Laptops and hand-held computers. The memory elements consume 70 percent of the total power in an IC. As flip-flops are the major sector of the memory elements used in any portable devices, the major concern to reduce the power consumption in flip-flops will help us to reduce the power consumption in an IC to a major extent. And reducing the number of clocked transistors give us good results in reduction of its power consumption. As flip-flops designed with conventional CMOS logic consume more power than flip-flops designed using transmission gates and pass transistors, and a gated flip-flops will reduce the un-necessary switching of transistors when the input and the output is same. Hence a gated flip-flop using transmission gate and pass transistors are used to reduce the average power consumption. In this paper a gated flip-flop is proposed and its power dissipation Vs input frequency results are compared w.r.t clocked pair-shared flip-flop (CPSFF). Tanner EDA tool is used with 180nm technology. Cadence EDA tool is used to design the layout.

Keywords- Pass transistor, Transmission gates, CPSFF, Power consumption

I. INTRODUCTION

Sequential circuits are the logic circuits whose outputs at any instance of time depend not only on the present inputs but also on the past outputs. Sequential circuits are of two types (i) synchronous or clocked and (ii) synchronous or un-clocked. The simplest kind of sequential circuit is a memory cell that has two states. It can be either 1 or 0. Such two state sequential circuits are called flip-flops because they flip-from one state to another and then flop back.

Flip-flops are used as the memory elements which are the basic building blocks of an IC. They are used in many applications like parallel data storage, shift registers, frequency division and counters etc. As synchronous flip-flops uses a master-clock generator, which generates a periodic train of clock pulses. This leads to huge power consumption of power in synchronous circuits. So, by eliminating the unnecessary switching of the transistors w.r.t clock signal in memory elements we can reduce the power dissipation to a Large amount. And also by avoiding un-wanted switching of internal transistors the power can be reduced. The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications. The power consumption in a circuit can be decreased by reducing:

• Switching activity in the circuit
• Switching capacitance of each node
• Supply voltage
• Short-Circuit Current

Now, the advantage of PTL comes from the fact that it is best suitable to implement all the above power reduction techniques:

1. Switching activity in the circuit can be reduced by eliminating the glitches. This can be done by controlling the delays of each pass transistor (controlling the widths and lengths).
2. Switching capacitance of a node in the PTL will be less when compared to a node in the CMOS design. Due to the smaller size of the transistors in PTL implementation.

• The lengths of the transistors should be as small as possible, because increased lengths result in more IR drop across the transistor.
• The widths of transistors also should be small. It’s because the improvement seen in the switching of that transistor will be subdued by the delay caused in the input, which is driving that wider gate.

3. Like the CMOS technologies, the supply voltage can be reduced at the cost of some increase in delay of the circuit.
4. There are fewer ground connections (only at the inverters) means fewer VDD to GND connections during switching. So theoretically PTL implementation should draw least amount of short circuit power.

So, the proposed gated D flip-flop has uses pass transistor and transmission gates unlike CMOS gated flip-flop like Clocked Pair Shared Flip flop (CPSFF).

II. CLOCKED PAIR-SHARED FLIP-FLOP (CPSFF)

CPSFF is a gated flip-flop which ensure efficient and robust implementation of low power sequential element, it uses less number of clocked transistor. The circuit diagram of CPSFF is shown below.
The short circuit power in CPSFF is dominant when input D is low and CLK is high, in order to achieve good power results we proposed a transmission gated D flip-flop.

III. PROPOSED CONDITIONAL DATA PASS TRANSISTOR FLIP-FLOP

In this model we used a XOR gate which is designed using a pass transistors to conditionally transmit the input to the flip-flop in order to avoid the unnecessary switching of the transistors in the flip-flop. If the input is same as output there we don’t pass the input to flip-flop instead we use a double inverted buffer at the output. The TG 1 indicated in the circuit will allow the input to pass only if it is different from the previous one, and TG 2 checks for the availability of the clock signal.

Figure 1: Circuit of Clocked Pair-Shared Flip-Flop (CPSFF)

Figure 2: XOR gate using pass transistor logic

Figure 3: proposed conditional data pass transistor flip-flop

Figure 4: proposed double edge-triggered conditional data pass transistor flip-flop

Figure 5: layout of proposed flip-flop in cadence

Figure 6: input and output waveforms w.r.t clock and supply voltage of proposed flip-flop
CONCLUSION AND RESULT

The power consumption of CPSFF and proposed pass transistor flip-flop are compared. It is observed at 50MHz clock frequency, and it is observed that flip-flop designed using pass transistor logic dissipates less power than CPSFF. Since there are fewer ground connections (only at the inverters) means fewer Vdd to GND connections during switching. At higher data rates this proposed flip-flop show irregular results, due to smaller pulse width of the input than the circuit delay. Work can be done to increase high data handling capability of proposed circuit. As the XOR gate used will be active for every transition, by reducing its threshold voltage can further decrease its power consumption.

REFERENCES