DESIGN OF VEDIC MULTIPLIER FOR COMPLEX NUMBERS FOR ENHANCED COMPUTATION USING VHDL

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Abstract- The main emphasis of this paper is to propose the design of 8 Bit Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. The work has proved the efficiency of Urdhva tiryakbhyam – Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased. The proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using EDA (Electronic Design Automation) tool – Xilinx9.1i. The main design features of the proposed system are the reconfigurability and flexibility

Keywords- Vedic multiplier, Urdhva tiryakbhyam, VHDL, EDA

I. INTRODUCTION

Multiplication is the process of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product addition to produce the final result [8]. Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. With time applications, many researchers have tried to design multipliers which offer either of the following- low power consumption, high speed, regularity of layout and hence less area or even grouping of them in multiplier.

The need of fast multiplication has gives rise to algorithms such as Baugh-Wooley method, Booth multiplier using recoding bits, Modified Booth algorithm (MBE). Although the MBE is most successful algorithms yet it is also a time consuming process. Nowadays, new methods are required for even faster multiplication strategies [5]. The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics [4]. By using this technique we can improve the computational speed of processor to perform fast arithmetic operations.

Vedic mathematics[2] is the name given to the ancient system of mathematics, or, to be precise, a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved – be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. Vedic mathematics was rediscovered from the ancient Indian scriptures between 1911 and 1918 by Sri Bharati Krishna Tirthaji (1884-1960), a scholar of Sanskrit, mathematics, history and philosophy [1]. He studied these ancient texts for years and, after careful investigation, was able to reconstruct a series of mathematical formulae called sutras.

Complex number arithmetic computation is a key arithmetic feature in modern digital communication and optical systems. Many algorithms based on convolutions, correlations, and complex filters require complex number multiplication, complex number division, and high-speed inner-products. Among these computations, complex number multipliers and complex number inner-products are becoming more and more demanded in modern digital communication, modern optical systems, and radar systems.

Multiplication is an essential operation for high speed hardware implementation of complex number computation. To compute the product of two complex numbers, the conventional method is to use four binary multiplications, one addition, and one subtraction. Define two complex numbers as:

\[ A = A_1 + jA_2 \text{ and } B = B_1 + jB_2 \]

Multiplication of A and B is given by

\[ AX = A_1B_1 - A_2B_2 + j(A_1B_2 + A_2B_1) \]

The paper is organized as follows. In section 2, Vedic multiplication method based on Urdhva Tiryakbhyam sutra is discussed. Section 3 deals with the design of the above said multiplier. Section 4 summarizes the experimental results obtained, while section 5 presents the conclusions of the work.
THE VEDIC MULTIPLICATION METHOD

The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on Urdhva Tiryakbhyam. The 16 sutras of Vedic mathematics [4] are given in the table 1, but the discussion of all the algorithms is beyond the scope of this paper.

II. URDHVA TIRYAKBHYAM SUTRA

The proposed Vedic multiplier is based on the “Urdhva Tiryagbhyam” sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and Crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products.

The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip.

The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

B. Multiplication of two decimal numbers 252 x 846

To illustrate this scheme, let us consider the multiplication of two decimal numbers 252 x 846 by Urdhva-Tiryagbhyaam method as shown in Fig. 1. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

III. THE PROPOSED MULTIPLIER ARCHITECTURE

The hardware architecture of 8x8 bit Vedic multiplier module is displayed in the below sections. Here, “Urdhva-Tiryagbhyaam” (Vertically and Crosswise) sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work.

Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 6 can be easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section. Let’s analyze 8x8 multiplications, say A= A7 A6 A5 A4 A3 A2 A1 A0 and B= B7 B6 B5 B4 B3 B2 B1 B0. The output line for the multiplication result will be of 16 bits as –S15 S14 S13 S12 S11 S10 S9 S8 S7 S6 S5 S4 S3 S2 S1 S0. Let’s divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH - AL. Similarly multiplicand B can be decomposed into BH - BL. The 16 bit product can be written as P = A x B = (AH - AL) x (BH - BL) = AH x BH + (AH x BL + AL x BH) + AL x BL

Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block a we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total three 8 bit Ripple-Carry Adders are required as shown in Fig. 2

![Fig. 1 Multiplication of two decimal numbers – 252 x 846](image1)

![Fig. 2 Block Diagram of 8x8 bit Vedic Multiplier](image2)
In this work, 8x8 bit Vedic multiplier is designed in VHDL (Very High Speed Integrated Circuits Hardware Description Language). Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in XilinxISE13.1i - Project Navigator and ISim simulator integrated in the Xilinx package.

In behavioural simulation we have tested for the following input bits:

a) For 8x8 bit Vedic multiplier input, the multiplier a="00000101" (decimal number system 5) and multiplicand b="00000110" (decimal number system 6) and we get 16-bit output1="0000000000011110" (decimal number system 30).

b) Again, we have multiplier a="00001000" (decimal number system 8) and multiplicand b="00000110" (decimal number system 6) with 16-bit output1="0000000000011000" (decimal number system 24).

In behavioural simulation we have tested for the following input bits:

a) For 8x8 bit Vedic multiplier input, the multiplier a="00000101" (decimal number system 5) and multiplicand b="00000110" (decimal number system 6) and we get 16-bit output1="0000000000011110" (decimal number system 30).

b) Again, we have multiplier a="00001000" (decimal number system 8) and multiplicand b="00000110" (decimal number system 6) with 16-bit output1="0000000000011000" (decimal number system 24).

**CONCLUSION**

This paper presents a highly efficient method of multiplication – “Urdhva Tiryakbhyam Sutra” based on Vedic mathematics. It gives us method for hierarchical multiplier design and clearly indicates the computational advantages offered by Vedic methods. The computational path delay for proposed 8x8 bit Vedic multiplier is found to be much lower than traditional multipliers. Hence our motivation is to reduce the delay. Therefore, we observed that the Vedic multiplier is much more efficient than Array and Booth multiplier in terms of execution time (speed). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education. In future, all the major universities may set up appropriate research centres to promote research works in Vedic mathematics.

**REFERENCES**


