VLSI IMPLEMENTATION OF LOW-COST FIR FILTER STRUCTURE BASED ON IMPROVED FAITHFULLY ROUNDED TRUNCATED MULTIPLIER

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Abstract – This paper presents the design of low-cost FIR filter structure based on Improved Faithfully rounded truncated multiplier. The Improved truncated multiplier design reduces the area and power consumption by computing the most significant part of Partial Product Bit (PPB) matrix and also minimizes the number of full adders and half adders used for compression of PPB matrix. In the proposed multiplier design, the least significant part of PPB matrix is significantly compressed by jointly considering deletion, truncation, and rounding. The total truncation error of improved truncated multiplier is not more than 1ulp (unit of least position) so this design gives the precised output. The FIR filter design is realized using improved truncated multiplier which achieves better area and power results. This design is simulated and synthesized using XILINX ISE software.

Keywords – Truncated Multiplier, Tree Reduction, Dsp Applications, Computer Arithmetic, Faithful Rounding.

I. INTRODUCTION

FIR (Finite impulse response) digital filter is basic component in many digital signal processing applications and communication systems. It is mostly used in many portable applications which require less area and power. In the FIR filter design, most of area and power consumption is by multipliers. In this paper we optimize the design of multipliers by using truncation process. Multipliers are basic building blocks of many high-speed systems such as digital signal processors, microprocessors, FIR filters, etc. The performance of the system is basically determined by the performance and the operation of multiplier because it is the slowest component in the system and more area consuming. Hence the optimization of area and speed of the multiplier is a big design issue.

Generally multiplication of two N-bit numbers results in 2N-bit product whereas in the truncated multiplication, only N-bit product result is generated by process of truncating the product result to required precision. Hence this results in reduction in area cost and the power consumption. There are also another subset of multipliers called fixed width multipliers which compute only N-most significant bits of 2N-bit product result and also makes use of extra compensation function or circuits to reduce the total truncation or rounding error.

There are two methods available for truncated multiplication and they are variable and constant corrections. Constant correction method calculates the average truncation error and then adds the row of constant into partial product bit matrix to compensate the error and to further reduce the total error, variable correction method is used. Hence the previous papers of truncated multiplier designs uses different compensation techniques to reduce various types of error.

In this paper, low-cost FIR filter structure is designed based on Improved faithfully rounded truncated multiplier design is presented with total truncation error less than 1ulp (unit of least position) and also this design jointly considers partial product reduction, truncation, rounding of partial product bit matrix. So that final product meets the precision requirements. Hence area occupied by FIR filter structure can be reduced significantly.

II. FIR FILTER DESIGN AND OPTIMIZATION

A digital FIR filter design consists of three steps and they are finding the filter order and coefficient, coefficient quantization, and hardware optimization. These three steps are shown in Fig. 1. In the first step, the filter order and its corresponding coefficients are determined in order to satisfy the frequency response specifications. Then in the second step, coefficient quantization is performed to quantize the coefficients to finite bit width accuracy. Finally hardware optimization is done to reduce the area and power consumption of hardware structure.

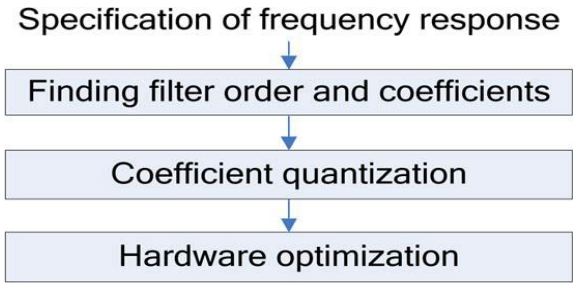

Fig. 1 Three stages in digital FIR filter design and implementation.

Hardware optimization is done by optimizing the design of multipliers used in FIR filter structure which occupies more area and consumes more power. Generally the design of parallel multipliers consists of following steps, i.e., partial product generation, partial product reduction, final carry propagate addition. In the first step, the partial products are generated from multiplicand and multiplier.

In the partial product reduction step, the generated partial products are compressed and reduced to two partial products and then they are finally added using final carry propagate adder. Already two famous reduction techniques available and they are Dadda tree and Wallace tree reduction [9]. In Dadda reduction, whenever compression operation is required the reduction is performed whereas in Wallace tree reduction, the partial product bits are always compressed.

There are two types of reduction schemes adopted in this paper called scheme-1 and scheme-2 reductions in order to reduce the number of half adders used in each column and also to perform flexible column-by-column reduction. By combining scheme-1 and scheme-2 reduction in the design of truncated multiplication, the area cost can be minimized.

III. TRUNCATED MULTIPLIER DESIGN

Truncated multiplication reduces power consumption by computing only the most significant bits of product result and most common approach used for truncation is physical reduction of partial product bit matrix. The main objective of improved faithfully rounded truncated multiplier design is to compute P most significant bits of the product with a total truncation error of not more than 1ulp, where 1ulp = 2^{-P}.

In the Existing design of truncated multiplication, there are three processes to remove the unnecessary Partial Product Bits (PPBs) and they are: deletion, truncation, and rounding. Two rows of partial product bits are set undeletable because they will be removed at the subsequent process of truncation and rounding. The two white dots at level 1 of reduction and the two white dots at level 2 of reduction are not generated during the process of compression with FAs or HAs. Thus, two simplified versions of the full adder (FA) and half adder (HA) cells are introduced, i.e., full adder and half adders without the sum output bits. For column T, the carry bit only is needed to be generated (to column T + 1) for the last full adder compression because the sum output bit will be discarded during the rounding process. For example, the FA compression does not need to generate the white dot (the sum output bit) at level 4 of reduction.

For column T + 1 to M + N, although Scheme 1 is adopted to determine whether an HA is needed or not, we actually do not compress the column height to one because this compression will cause ripple carry. Indeed, at the last level of the reduction process, some column, for example column i, has a height of three, and the remaining columns beyond this specific column, i.e., columns i + 1, i + 2, . . .etc have a column height of two, as shown in level 4 of Fig. 2(a). Finally compressed partial product bits are added using final carry propagate adder.

A. Improved Truncated Multiplier Design

The improved design of faithfully rounded truncated multiplier is shown in Fig. 2(b) where the gray circles, crossed green circles, and crossed red circles represent the deleted bits, truncated bits, and rounded bits respectively. Only a single row of partial product bits (PPBs) is made undeletable for the subsequent rounding, and the partial product bit elimination consists of only deletion and rounding.

The deletion and rounding error ranges (E_D' and E_R') in the improved design of truncated multiplication are given in Equation as follows,

$- ulp \leq E_D' \leq 0$

$- ulp \leq E_R' \leq 0$

$-1/2ulp \leq E_D = E_D' + 1/2\ ulp \leq 1/2\ ulp$

$-1/2ulp \leq E_R = E_R' + 1/2\ ulp \leq 1/2\ ulp$

$-ulp \leq (E_D + E_R) \leq ulp$

From the above ranges of error, the deletion error in the improved design is twice greater than that in existing truncated multiplier design. Hence in the improved design more partial product bits (PPBs) can be deleted which leads to smaller area in the subsequent partial product bit compression.

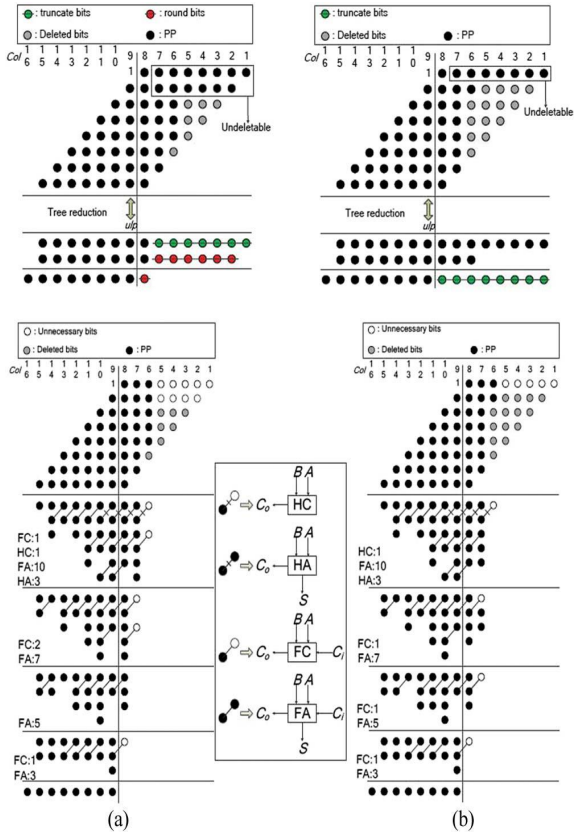

Fig. 2 Truncated Multiplier design (a) Existing design (b) Improved design.

B. Proposed Truncated Design Output

The simulation and synthesis result of improved faithfully rounded truncated multiplier design is shown in the Fig. 3 & 4 and Xilinx ISE software is used to simulate and synthesis the proposed design.

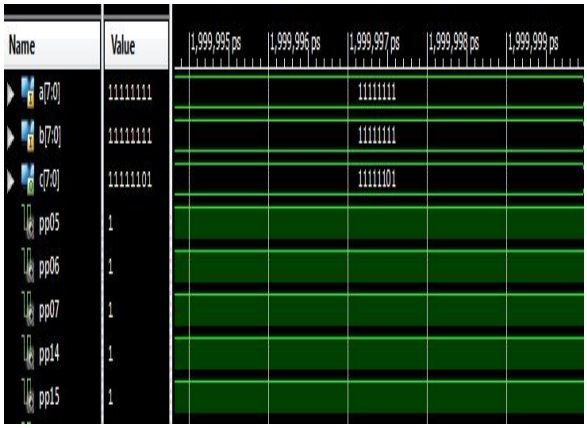

Fig. 3 Simulation result of proposed faithfully rounded truncated multiplier

Number of Slices:	55	out of 768	7%
Number of 4 input LUTs:	96	out of 1536	6%
Number of IOs:	24		
Number of bonded IOBs:	24	out of 124	19%

Fig. 4 Synthesis results of proposed truncated multiplier

Thus 8-bit truncated output is obtained from proposed new truncated multiplier and in this design, area used is less compared to the existing truncated multiplier and this design slightly increases error compared to existing one but still optimal for using in low-cost DSP applications. Hence we apply this improved truncated multiplier in the design of FIR filter.

IV. REALIZATION OF FIR FILTER USING IMPROVED TRUNCATED MULTIPLIER

The improved truncated multiplier is effectively used in the design of direct form FIR filter structure. In Conventional FIR filer structure, general multiplication of input and coefficient is performed without considering the length. Thus in order to meet precision requirement and for the design to be within the architecture bit width, FIR filter structure is implemented using the new improved faithfully rounded truncated multiplier so that area cost can be reduced significantly.

FIR filter structure performs weighted sum of input sequences called as convolution sum which are used to implement low-pass, band-pass, or band-pass filter structures which satisfy their respective frequency response. The power consumption and computations used in FIR filter is directly proportional to filter order. So if the filter order can be changed dynamically, the number of multipliers used in FIR filter can be reduced leading to small area in the design. The architecture of FIR filter implementation using improved truncated multiplication is shown in Fig. 5. In this paper, direct form FIR filter structure is designed because transpose form structure occupies more area compared to direct form structure.

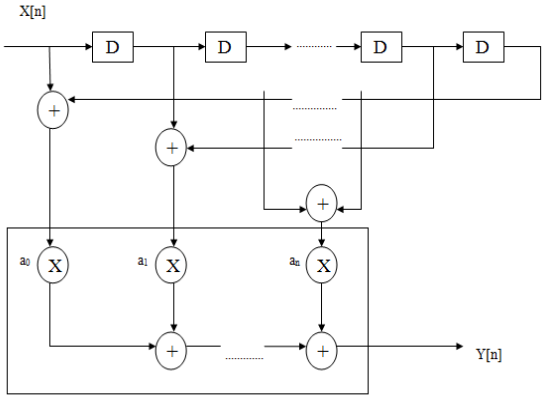

Fig. 5 Architecture of FIR filter implementation using improved truncated multiplication

The architecture of FIR filter has MCMA (Multiple Constant Multiplication/Accumulation) represented in rectangle box is used to perform concurrent multiplications of input and their coefficients and finally all products are accumulated and added using carry propagate adder.

V. RESULTS AND DISCUSSION

The simulation result of FIR filter structure using improved truncated multiplier design is shown in Fig. 6.

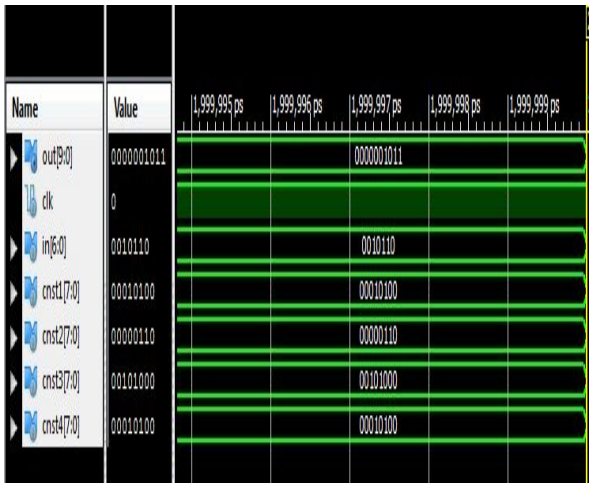

Fig. 6 Simulation result of FIR filter using improved truncated multiplier

This design is simulated and synthesized using XILINX ISE. The coefficients are stored in the ROM as they are fixed. The output changes with respect to the CLK signal. The power of the FIR filter structure is analyzed by using XILINX power analyzer. The power calculated with respect to the CLK.

TABLE I COMPARISON OF SYNTHESIS RESULT OF FIR FILTER USING EXISTING AND IMPROVED TRUNCATED MULTIPLIER

PARAMETERS: Number of	EXISTING DESIGN	PROPOSED DESIGN
Slices	447 out of 768 58%	295 out of 768 38%
Slice Flip Flops	56 out of 1536 3%	56 out of 1536 3%
4 Input LUTS	748 out of 1536 48%	476 out of 1536 30%
IOs	52	50
Bonded IOBs	51 out of 124 41%	50 out of 124 40%
GCLKs	1 out of 8 12%	1 out of 8 12%

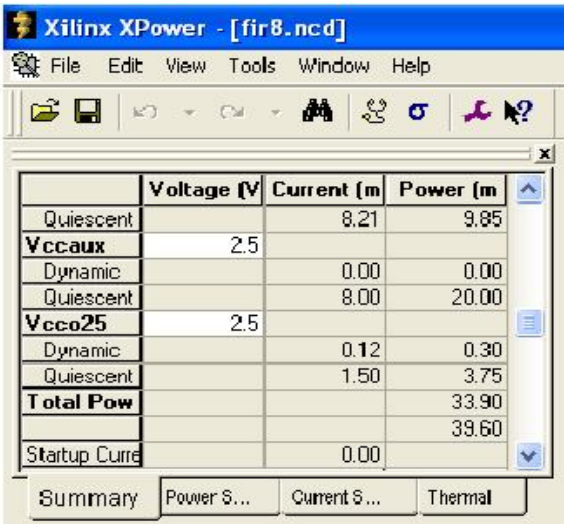

Fig. 8 Power analysis results of FIR filter

From the above results, FIR filter structure using improved truncated multiplier occupies less area and delay and power consumption is minimized in this structure compared to existing FIR filter design

CONCLUSION

This proposed paper discussed and elaborated the design of low-cost FIR filter structure based on improved faithfully rounded truncated multiplier. FIR filter design steps and hardware optimization using truncated multiplication are mainly discussed. The improved truncated multiplier design reduces the area and power consumption by computing MSB part of PPB matrix.

The proposed new truncated multiplier occupies less area compared to the existing design. Thus improved truncated multiplier is used in the design of direct form FIR filter structure and the filter design is analyzed in terms of area, power and delay which show significant reduction of them leading to low-cost FIR filter structure.

REFERENCES

[1] Manuel de la Guia Solaz, WeiHan,RichardConway, "A Flexible Low Power DSP With a Programmable Truncated Multiplier", in IEEE transactions on circuits and systems-I: regular papers, 2012, vol. 59, no. 11, p.2555-2568.

[2] shen-fu hsiao, jun-hong zhang jian, and ming-chih chen, "low-cost fir filter design based on faithfully rounded truncated multiple constant multiplication/accumulation", in IEEE transactions on circuits and systems-II: express briefs, 2013, vol. 60, no. 5, p.287-291.

[3] J.-P. Wang, S.-R. Kuang, and S.-C. Liang, "High-accuracy fixed-width modified booth multipliers for lossy applications", in IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2011, vol. 19, no. 1, p.52-60.

[4] Nicola Petra, Member, IEEE, DavideDe Caro, Senior Member, IEEE, Valeria Garofalo, Ettore Napoli, and Antonio Giuseppe Maria Strollo, Senior Member, IEEE, "Design of Fixed-Width Multipliers With Linear Compensation Function", in IEEE transactions on circuits and systems-I: regular papers, 2011, vol. 58, no. 5, p.947-960.

[5] Shiann-Rong Kuang, Member, IEEE, and Jiun-Ping Wang, "Design of Power-Efficient Configurable Booth Multiplier", in IEEE transactions on circuits and systems-I: regular paper, 2010, vol. 57, no. 3, p.568-580.

[6] N. Petra, D. De Caro, V. Garofalo, E. Napoli, and A. G.M. Strollo, "Truncated binary multipliers with variable correction and minimum mean square error", in IEEE Trans. Circuits Syst. I, Reg. Papers, 2010, vol. 57, no. 6, p.1312-1325.

[7] Valeria Garofalo, Nicola Petra, Member, IEEE, and Ettore Napoli, "Analytical Calculation of the Maximum Error for a Family of Truncated Multipliers Providing Minimum Mean Square Error", in IEEE transactions on computers, 2011, vol. 60, no. 9, p.1366-1371.

[8] Chip-Hong Chang and Ravi Kumar Satzoda, "A Low Error and High Performance Multiplexer-Based Truncated Multiplier", in IEEE transactions on very large scale integration (VLSI) systems, 2010, vol. 18, no.12, p.1767-177.

[9] Ron S. Waters, Member, Earl E. Swartzlander, "A Reduced Complexity Wallace Multiplier Reduction", in IEEE transactions on computers, 2010, vol. 59, no. 8, p.1134-1137.

[10] H.-J. Ko and S.-F. Hsiao, "Design and application of faithfully rounded and truncated multipliers with combined deletion, reduction, truncation, and rounding", in IEEE Trans. Circuits Syst. II, Exp. Briefs, 2011, vol. 58, no. 5, p.304-308.

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