A CASCADED MULTILEVEL CONVERTER WITH REDUCED COMPONENTS APPLIED TO INDUCTION MACHINE DRIVE

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Abstract – Today, the industrial trend is moving away from heavy and bulky components to power converter systems that use more and more semiconductor elements controlled by powerful processor systems. However, it is difficult to connect traditional converters to the high and medium voltage grids, as a single power electronic switch cannot stand at high voltage. By considering these reasons, a new family of multilevel converters has appeared. The main objective of the work is to improve the multilevel converter topologies for high quality and high power applications by reducing the number of components. The proposed topology, not only has the lower number of components, but also the full-bridge converters operate at lower voltage. A three phase 49-level cascaded multilevel converter is developed which is applied to the induction motor drive & is validated through Matlab/Simulink platform.

Keywords: Full bridge topology, multilevel converter, sub multilevel converter.

I. INTRODUCTION

The concept of multilevel converter was introduced by Nabae in 1975. The term multilevel began with the three level converters. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. Multilevel converters have been used for medium-to-high voltage applications such as large electric drives, reactive power compensations and FACTS devices. The H-bridge topology was followed by the diode-clamped converter [1]. The diode-clamped converter utilized a bank of series capacitors. But, they need an excessive number of clamping diodes for a high number of voltage levels [2]. J. Rodriguez, J. S. Lai and F. Z. Peng gives overview on various types of inverter topologies and the most relevant control and modulation method developed for the family of converters. Another fundamental multilevel topology, the flying capacitor [3], involves series connection of capacitor clamped switching cells. This topology has several attractive properties when compared to the diode-clamped converter, including the advantage of transformer less operation [4] and [5]. But, for a high number of voltage steps it requires excessive number of storage capacitors. The cascaded H-bridge topologies [6] are good solution for high-voltage applications due to the modularity and the simplicity of control. But, it requires a large number of separated voltage sources to supply each conversion cell. In [6], the author presents a new multilevel voltage source inverter with separate dc sources. This inverter can generate almost sinusoidal waveform voltage with only one time switching per cycle as the number of levels increases and also it can solve the size and weight problems of multilevel converters. An attempt has been made in [7] and its development in [8] and [9] to introduce a new topology for multilevel converters with a reduced number of components but, the switches used in these topologies operate at the peak of the output voltage. Therefore, a bulky and costly interface transformer needs to be used for high-voltage applications. E. Babaei gives overview on a new multilevel converter topology that has many steps with fewer power electronic switches. This presents a new algorithm for determination of magnitudes of different dc voltage sources. It results in reduction of the number of switching losses, installation area and cost of the converter. But, the converter needs a large number of bidirectional switches and the blocking voltage of bidirectional switches is also high. The proposed topology is compared with two other topologies recommended in [7] and [8] in terms of number of IGBTs, blocking voltages on switches and losses of switches. Hence the work may be extended on implementing either by changing the technique of triggering to the switches or closed loop control with suitable harmonic elimination technique to achieve better performance of the converter. In [10], the author presents a new topology of cascaded multilevel converter to overcome aforementioned disadvantages. It is based on the cascaded connection of single phase sub multilevel converter units and it produces a large number of steps with a low number of power switches and components. Hence it significantly reduces the number of dc voltage sources, switching devices, installation area and converter cost.

II. DESIGN TOPOLOGY

The circuit diagram of the proposed sub multilevel topology circuit as shown below.
The proposed topology for a sub multilevel converter is shown in Figure 3, which consists of the basic unit and a full bridge converter. The basic unit consists of \( n \) dc voltage sources. Each dc voltage source is connected to the output by two switches and can produce a zero or positive polarity voltage. And each switch is composed of an Insulated Gate Bipolar Transistor with an anti parallel diode. A positive polarity staircase waveform has been produced by the basic unit. The output side of the basic unit is connected to a single-phase full-bridge converter, which alternates the input voltage polarity and provides a positive or negative staircase waveform at the output and the full-bridge converters operate at a lower voltage. This extends the applications of the proposed cascaded multilevel converter for high voltages. The switches used in this basic unit and full-bridge are complementary controlled. For simplicity, just neglect the on-state voltage drops of the switches.

As can be seen, \( 2^{n+1} - 1 \) different values can be obtained for \( v_o \).

### III. CIRCUIT OPERATION

The basic unit of the sub multilevel converter is shown in Fig. 1. The cascaded connection of this sub multilevel converter increases the possible value of \( v_o \), effectively. But, it can only generate the positive output voltages. The full-bridge converter is connected to the output of the basic unit, which provides a positive or negative staircase waveform.

The typical output waveforms of \( v_o \) and \( v_o' \) are shown in Fig. 1(b).

\[
v_o = v_{o1} + v_{o2} + \ldots + v_{ok}.
\]

### IV. METHODOLOGY OF THE CONVERTER

<table>
<thead>
<tr>
<th>State</th>
<th>Switches States</th>
<th>( v_o' )</th>
<th>( v_o )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>off off \ldots off on off</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>on off \ldots off off off</td>
<td>( v_2 )</td>
<td>( -v_2 )</td>
</tr>
<tr>
<td>3</td>
<td>on off \ldots on off on</td>
<td>( v_3 )</td>
<td>( -v_3 )</td>
</tr>
<tr>
<td>4</td>
<td>off on \ldots off off off</td>
<td>( v_4 )</td>
<td>( -v_4 )</td>
</tr>
<tr>
<td>5</td>
<td>off on \ldots on on on</td>
<td>( v_5 )</td>
<td>( -v_5 )</td>
</tr>
<tr>
<td>( 2^m )</td>
<td>off off \ldots on off on</td>
<td>( v_{m} )</td>
<td>( v_{m} )</td>
</tr>
<tr>
<td>( 2^m+1 )</td>
<td>on off \ldots off off off</td>
<td>( v_{m+1} )</td>
<td>( v_{m+1} )</td>
</tr>
<tr>
<td>( 2^m+2 )</td>
<td>on on \ldots off off off</td>
<td>( v_{m+2} )</td>
<td>( v_{m+2} )</td>
</tr>
<tr>
<td>( 2^m+3 )</td>
<td>on on \ldots on off off</td>
<td>( v_{m+3} )</td>
<td>( v_{m+3} )</td>
</tr>
</tbody>
</table>

Table 1: List of Values of \( v_o \) for different states of the switches.
Table 1 shows the voltage levels and their corresponding switch states. For an example, an output voltage level \( v_o = 0 \) by turning on devices \( T_{11}, T_{21}, S_{11}, S_{12}, S_{21}, S_{22}, T_{12}, T_{22} \). By turning on devices \( S_{11}, S_{21}, S_{12}, S_{22}, T_{12}, T_{22}, T_{11}, T_{21} \), yields \( v_o = 30V \). For an output voltage \( v_o = -30V \) by turning on devices \( S_{11}, S_{21}, S_{12}, S_{22}, T_{12}, T_{22}, T_{11}, T_{12} \). The proposed converter requires 16 switching devices and 4 dc voltage sources to produce an output voltage as 230V and it is able to generate 49 steps in the output. The other hand the cascaded multilevel converter with reduced switches requires 22 switching devices and 6 dc voltages to provide an output voltage as 230V and it is able to generate 53 steps in the output. When all the dc voltage sources take the different value, then the proposed converter has less number of components compared to the conventional cascaded converter.

V. EVALUATION OF MAGNITUDES OF DC VOLTAGE SOURCES

Asymmetrical structures can be used for providing a large number of output steps without increasing the number of inverters. In this topology, the magnitudes of dc voltage sources are determined in order to have unequal values for \( V_o \) and produce linear steps. For producing all steps in the output, the normalized values of the dc voltage sources must be chosen using the following procedure:

For unit 1:

\[
V_{11} = 2V_{dc}, \quad i = 1...n_1
\]

(2)

\[
V_{ii} = 2V_{11} = 2V_{dc}, \quad i = 2...n_1
\]

(3)

For unit 2:

\[
V_{21} = V_{11} + 2\sum_{j=1}^{n_1} V_{ij} = (4n_1 -1)V_{dc}
\]

(4)

\[
V_{22} = 2V_{21} = 2(4n_1 -1)V_{dc}, \quad i = 2...n_2
\]

(5)

In general, for the mth unit:

\[
v_{m1} = V_{11} + 2\sum_{j=1}^{n_1} \sum_{i=1}^{n_1} V_{ij} = 2\prod_{j=1}^{m-1}(4n_j -1)V_{dc}
\]

(6)

\[
v_{mi} = 2V_{m1} = 2\prod_{j=1}^{m-1}(4n_j -1)V_{dc}, \quad i = 2...n_m
\]

(7)

The maximum output voltage is evaluated by the following equation:

\[
v_{omax} = \sum_{i=1}^{n} 2\prod_{j=1}^{m}(2n_i - 1) \times V_{ii}
\]

(8)

The number of generated steps in the output voltage is expressed by the following equation:

\[
N_{step} = 2 \prod_{i=1}^{m}(4n_i - 1)
\]

(9)

VI. TEST SYSTEM

Case 2: Three phase cascaded multilevel converter applied to induction machine drive. The simulation circuit of three phase cascaded multilevel converter applied to induction machine drive is shown below. Three phase induction motors are widely used in industrial drives because they are rugged, reliable and economical.

![Fig. 4: Block diagram of a cascaded multilevel converter which is applied to induction machine drive.](image1)

![Fig. 5: Simulink model of single phase 49-level cascaded multilevel converter.](image2)

![Fig. 6: Simulink model of three phase cascaded multilevel converter applied to induction machine drive.](image3)
VII. RESULTS AND DISCUSSIONS

The simulation results of single phase 49-level cascaded multilevel converter shows the output voltage of first basic unit in fig.7 and second basic unit in fig.8, the output voltage of first sub multilevel converter in fig.9, output voltage of second sub multilevel converter in fig.10 and overall output voltage and current of the converter in fig.11 & 12 with a peak amplitude of 240V and 2.2A. The output voltage of each basic unit has always a zero or a positive value. The ac outputs of the full-bridge converter have been connected in series such that the synthesized voltage waveform is the sum of outputs of full-bridge converters. There is a phase difference between the output voltage and current waveforms, which is due to the inductive characteristic of the load. Since the load of the converter is almost a low pass filter, the output current contains less high order harmonics than the output voltage.

Fig. 7: Output voltage of first basic unit
Fig. 8: Output voltage of second basic unit
Fig. 9: Output voltage of first sub multilevel converter
Fig. 10: Output voltage of second sub multilevel converter
Fig. 11: Overall output current of the converter
Fig. 12: Overall output voltage of the converter
Fig. 13: Stator current, Speed and Torque of induction machine drive
The simulation results of three phase cascaded multilevel converter applied to induction machine drive is shown in fig.13. A single phase 49-level cascaded multilevel converter is converted into a three phase 49-level cascaded multilevel converter by using transport delay block. The output of the cascaded multilevel converter is given to the input of the induction machine drive having an voltage with peak amplitude of 240V.

CONCLUSION

A single phase 49-level cascaded multilevel converter and the three phase cascaded multilevel inverter applied to induction machine drive with a reduced number of switching devices and dc voltage sources have been simulated by using MATLAB/SIMULINK. It is based on the cascaded connection of sub multilevel converters. And the structure extends the design flexibility and possibilities to optimize it for various objectives. Asymmetrical cascaded multilevel converter uses least number of devices to produce higher voltage level. It has been shown that the proposed topology generate 49 steps on the output voltage with a peak of 240V, using 16 IGBTs, 4 dc voltage sources and blocking voltage of 960V. But, the other topology [7] produces 53 voltage steps using 22 IGBTs, 6 dc voltage sources and blocking voltage of 1674V. The proposed topology not only has lower number of components, compared to the other topologies, but also the full-bridge converters operate at a lower voltage. This extends the applications of the proposed converter for high voltages.

REFERENCES


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