COMBINED NON-ISOLATED HIGH STEP-UP BOOST CONVERTER AND SEPIC CONVERTER APPLIED TO INDUCTION MOTOR

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Abstract— A general Boost converter has a disadvantage that it has limited voltage step-up ratio because of its parasitic resistance and also for high voltage applications it requires a high voltage rating diode which causes serious reverse recovery problems, which results in low step up ratio and low efficiency, so a non-isolated high step-up boost converter combined with an isolated sepic converter is developed in this paper to satisfy both high efficiency and high conversion ratio which does not need a current snubber for the diodes and is applied to an induction motor using MATLAB platform.

Keywords: Sepic converter, Boost converter.

I. INTRODUCTION

They are many DC-DC converters like Buck, Boost, Buck-Boost, Forward, and Sepic. A Boost converter is one of the DC-DC converters which step-up the input voltage, but it can’t satisfy both high voltage conversion ratio and high efficiency at once this is because of its parasitic resistance, which causes serious degradation in step-up ratio and efficiency as the operating duty increases. Also in high voltage applications a high voltage rating diode causes severe reverse recovery problem, which requires a snubber circuit [2]-[4] that results in more losses. Thus a general boost converter cannot be used for high step-up applications. In order to overcome these difficulties various types of step-up converters, a coupled inductors and a multiplier cell can be adopted [5]-[10]. Current-fed converters can offer high step-up ratio which can be used for high step-up applications using multiple switches [5], [11]. But it requires a snubber circuit to limit the voltage spikes which results in more losses. To overcome this problem active clamp method can be used which reduces switching losses, but its structure is complex as it contains more number of switches. Boost converter along with coupled-inductor can also be used for low-to-medium power applications, but it requires an auxiliary circuit to control switching voltage spikes [6]-[8]. A switched capacitor or a voltage multiplier can also be used [9]-[10], but it requires more number of capacitors and diodes resulting in complexity of structure. To obtain high step up ratio a classical boost converter can be combined with an isolated converter as a series output module. A boost converter combined with an isolated sepic converter as series module is developed as shown in Fig. 1, to satisfy high step-up voltage ratio and high efficiency. It is more efficient than any other types of converter as it provides an additional step-up ratio and a distributed voltage stress on devices, maintaining the advantage of boost converter. A boost converter and an isolated sepic converter can be easily integrated as they share some common parts as shown in Fig1. Fig. 2 represents the circuit of sepic integrated boost converter. C.J Tseng and C. L.Chen tells that a passive snubber cell is required to improve the turn on and turn off transients of the MOSFET’s in non-isolated pulse width modulated (PWM) dc/dc converters. Switching and EMI losses can also be reduced [2]. K. M. Smith and K. M. Smedley derives general topologies and electrical properties which are common to all lossless passive soft-switching converters with defined characteristics and proposed a synthesis procedure for creation of new converters [3]. In Boost converter with coupled inductors and buck-boost type of active clamp [6] T. F. Wu, Y. S Lai, J. C. Hung, and Y. M. Chen proposes a boost converter with coupled inductors and a buck–boost type of active clamp which uses an active- clamp circuit to eliminate voltage spike. From high efficiency high step-up dc-dc converters Q. Zhao and F. C. Lee proposed some dc-dc converters provide high step up voltage gain but along with extreme duty ratio or high circulating energy. So a high efficiency, high-step up dc-dc converter is designed to overcome this problem but it contains more switches which results in complex structure [7]. M. Prudente, L. L. Pfischer, G. Emmendoerfer, E. F. Romaneli, and R. J. Gules derived the use of voltage multiplier cell technique applied to a dc converter to obtain high step up static gain, reduction of maximum switching voltage, zero-current switching on time but it requires more number of capacitors and diodes and besides it requires a current snubber to reduce the reverse recovery on diodes [9].

II. CIRCUIT OPERATION AND MATHEMATICAL MODELLING

Fig.1. Combining of Boost converter and isolated Sepic converter
For the operation of Sepic integrated boost converter, we consider many assumptions, transformer T is modeled as magnetizing inductor $L_m$, a leakage inductor $L_{kg}$, and an ideal transformer with turn ratio $n$. $V_a$ as input voltage, $V_{cb}$ as balancing capacitor voltage, $V_{o1}$ as lower module output voltage, $V_{o2}$ as upper module output voltage which are considered as constant. The switch and diode are considered as ideal. The operation of Sepic integrated boost converter includes the combined operation of boost and Sepic converter with common switch and boost inductor. It can be operated in two modes i.e. for $n > 1$ and $n < 1$. In this paper we are considering $n > 1$. Fig.3 shows the key waveforms for $n > 1$.

As shown in Fig.3, one period is divided into four modes. Before $t_0$, boost inductor current $I_{lb}$ and transformer magnetizing current $I_{lm}$ flow through $D_{o2}$. The topological states for $n > 1$ are shown in Fig.4 (a)-(d).

**4(a) Mode1 [$t_0$ -$t_1$]**: Switch Q is turned on at $t_0$. As $D_{o2}$ is still conducting the entire voltage $V_{cb} + V_{o2}/n$ is impressed on transformer leakage inductor $L_{kg}$. Thus transformer primary current $I_{km}$ increases linearly. Therefore $I_l$ increases and $I_{D02}$ decreases accordingly resulting in commutation between $I_l$ and $I_{D02}$. As $L_{kg}$ provides current snubbing effect, the reverse recovery of $D_{o2}$ can be reduced and $D_{o1}$ is reverse biased by $V_{o1}$.

**4(b) Mode2 [$t_1$ -$t_2$]**: At $t_1$ current $I_{D02}$ reaches to zero and both $I_{lb}$ and $I_{lm}$ currents flow through switch Q. $L_{kg}$ contains only $I_{lm}$. $V_c$ and $V_{cb}$ are applied to $I_{lb}$ and $I_{lm}$ respectively. Thus $I_{lb}$ and $I_{lm}$ are increased linearly. $V_{cb}$ is reflected to the secondary side of the transformer, thus $D_{o2}$ is reverse biased by $nV_{cb} + V_{o2}$. Mode3 [$t_2$ -$t_3$]: At $t_2$ switch Q is turned off and the currents $I_{lb}$ and $I_{lm}$ flow through $D_{o1}$. Since $L_{kg}$ prevents the current flowing from $D_{o2}$, $V_0$ is clamped to $V_{o1}$. $V_c - V_{cb}$ and $-V_{o2}/n$ are applied to $I_{lb}$ and $I_{lm}$. Thus $I_{lb}$ and $I_{lm}$ are decreased linearly. Meanwhile $D_{o2}$ starts to conduct and $V_{cb} + V_{o2}/n - V_{o1}$ is impressed on $L_{kg}$, forcing $I_{kg}$ to decrease slowly. As $I_{kg}$ is decreased, $I_{D01}$ is decreased and $I_{D02}$ is increased linearly. Since $D_{o1}$ has a gentle slope, the reverse recovery of $D_{o1}$ can be decreased. Mode4 [$t_3$ -$t_4$]: At $t_3$, $D_{o1}$ reaches to zero and the currents $I_{lb}$ and $I_{lm}$ flow through $D_{o2}$. $D_{o1}$ is blocked by $V_{o1} - V_{cb} - V_{o2}/n$ and $V_c - V_{cb} - V_{o2}/n$ is applied to $I_{lb}$. Therefore $I_{lb}$ is decreased slowly than in mode 3. The current waveform is simplified for the purpose of analysis as shown in Fig.5, and here we assume that $D_{o1}T_0$ is zero and $I_{lb}$ and $I_{lm}$ are assumed as constant. Average value is represented by $(.)$.
The current stress on switch is equal to the sum of magnetizing inductor current and boosts inductor current which is same as \( I_{D_{01}} \) as in (j).

\[
I_{Q\text{-peak}} = I_{D_{01\text{-peak}}} = I_{Lb} + I_{Lm}
\]

\[
= \frac{1+n+D}{1-D}I_0 = (\frac{1+n+D}{1-D})I_{in}
\]

Similarly the current stress on \( D_{02} \) is equal to sum of \( I_{Lb} \) and \( I_{Lm} \) in the secondary as shown in (k).

\[
I_{D_{02\text{-peak}}} = \frac{1}{n}(I_{Lb} + I_{Lm}) = \frac{1}{n}\frac{1+n+D}{1-D}I_0
\]

The voltage stress on \( D_{02} \) at steady state is \( nV_{cb} + V_{o2} \), if the voltage ringing is ignored and is expressed as in (l).

\[
V_{D_{02\text{-peak}}} = nV_{cb} + V_{o2} = nV_s + V_{o2} = \frac{V_{o2}}{D}
\]

Diode Junction Capacitance Effect: For previous analysis we have considered the switch and diode as ideal devices, so that intrinsic capacitors are not considered. But in real operation they affect the working of the circuit. The circuits and waveforms considering the intrinsic capacitor are shown in Fig. 6. Between the intervals \( t_0 \sim t_1 \) voltage \( V_{cb} + V_{o2}/n \) is applied to \( L_{02} \). When \( I_{D_{02}} \) reaches zero at \( t_1 \), the voltage \( V_{cb} + V_{o2}/n \) is impressed on resonant circuit as shown in Fig. 6(b), thus \( \frac{1}{C_{ij2}} \) is the reflected \( C_{ij2} \) to the primary.

The average current of \( I_{Lb} \) is the same as the average input current \( I_{in} \) as in (h)

\[
(I_{Lb}) = I_{in} = \frac{1+nD}{1-D}I_s
\]

And also the average current of \( I_{Lm} \) is same as the output current as in (i).

\[
(I_{Lm}) = \frac{n(1-D)I_s}{1+nD} = nI_0
\]
turns off at \( t_2 \) the circuit will be as shown in Fig. 6(c). Here the effect of \( I_{Lb} \) will be small and the currents \( I_{Lb} \) and \( I_{Lm} \) are considered as current sources, \( C_{oss} + C_{11} \) as charge and \( n_{Q2} \) as discharge. Thus the charging/discharging currents are divided according to the ratio of capacitance. Due to this some drop current, \( I_{drop} \) as in Fig. 6(a), is occurred on \( I_{Lb} \) as \( I_{Lb} + I_{Lm} \) is flowing through \( I_{Lkg} \). Diode voltage-stress distribution methods From equation (i) it is observed the voltage stress across \( D_{02} \) is higher than \( V_{02} \), thus it requires a high voltage rating diode which results in high cost and also low performance in high-output voltage applications. There are two methods to distribute the diode voltage stress; they are multiwinding structure as shown in Fig. 7 and clamp diode employed structure as shown in Fig. 8.

The clamp diode employed structure is simple non dissipative method, that contains two auxiliary diodes \( d_{a2} \) and \( d_{a3} \) which are to be employed in series with the two main diodes \( D_{02} \) and \( D_{03} \) in parallel to \( V_{02} \) as shown in Fig. 8. When the voltage ringings across the main diodes reaches \( V_{02} \) the clamping diodes get conducted, thus \( V_{02} \) and \( V_{03} \) are limited by \( V_{02} \). As small ringing current flows through clamp diodes low-current rating diodes can be used. For the proper function of this method it should satisfy the condition \( V_{02} > nV_{Ch} \).

### III. TEST SYSTEM AND DATA

#### Table 1- Input data required for Sepic integrated Boost converter

<table>
<thead>
<tr>
<th>PART</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage ( V_i )</td>
<td>42v</td>
</tr>
<tr>
<td>Output voltage ( V_o )</td>
<td>400v</td>
</tr>
<tr>
<td>Output power ( P_o )</td>
<td>200W</td>
</tr>
<tr>
<td>Switching Frequency ( f_s )</td>
<td>60KHz</td>
</tr>
<tr>
<td>Boost inductor ( L_b )</td>
<td>618\mu F</td>
</tr>
<tr>
<td>Transformer turn ratio</td>
<td>5</td>
</tr>
<tr>
<td>Balance capacitance ( C_b )</td>
<td>11\mu F</td>
</tr>
</tbody>
</table>

![Fig. 9 Block diagram of Sepic integrated Boost converter applied to induction motor](image)

![Fig. 10 Simulink model of Sepic combined Boost converter applied to induction motor with an input of about 42v.](image)

### IV. RESULTS AND DISCUSSIONS

The simulation is carried for Boost converter, Sepic integrated boost converter and Sepic integrated Boost converter applied to induction motor:

1. Boost converter with an input of 42v.
2. Sepic combined Boost converter with an input of 42v.
3. Sepic combined Boost converter applied to induction motor

![Fig. 11 output voltage of boost converter](image)
integrated Boost converter with the same input of 42v and resistive load of 800Ω. Fig 13 represents the waveforms of speed and electromagnetic torque of induction motor with an input of 400v from Sepic integrated Boost converter which is inverted by cascade h-bridge. Thus from Fig. 11 and Fig 12(d) we can see that for the same input of 42v for both boost converter and sepic integrated boost converter the output voltage highly varies resulting in high conversion ratio.

**CONCLUSION**

A sepic integrated boost converter is applied to induction motor is developed in this paper. Here an input of 42v is applied for a general boost boost converter which gives an output of 82v, where as in case of sepic integrated boost converter it gives an output of 400v fpr the same input of 42v. Thus it is applicable for non-isolated high step up applications with high step-up ratio along with the advantages of boost converter. A converter with boost inductor and switch as input stage can also be integrated with converter similar to sepic integrated boost converter.

**REFERENCES**


