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FPGA IMPLEMENTATION OF PARTIAL DISCHARGE DETECTION TO COUNT PD SIGNALS FOR HV APPLICATIONS

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Abstract- A partial discharge (PD) is the dissipation of energy caused by the buildup of localized electric field intensity. In high voltage devices such as transformers, this buildup of charge and its release can be symptomatic of problems associated with aging, such as floating components and insulation breakdown. This is why PD detection is used in power systems to monitor the state of health of high voltage transformers. If such problems are not detected and repaired, the strength and frequency of PDs increases and eventually leads to the catastrophic failure of the transformer, which can cause external equipment damage, fires and loss of revenue due to an unscheduled outage. FPGA technology is being widely used for fast digital processing capability. The research shall involve ISE Simulator version 9.2i Xilinx and VHDL programming to evaluate the use of FPGA for the detection and counting of PD signals in HV applications. The impulse signals will be processed, detected and counted using ADC with peak detector and counter.

Keyword- Partial Discharge Detection, FPGA Simulation, FPGA Technology, ADC with Peak Detector Block, Real Time Processing, Underground Cable, Counter with Reset Block, VHDL Programming.

I. INTRODUCTION

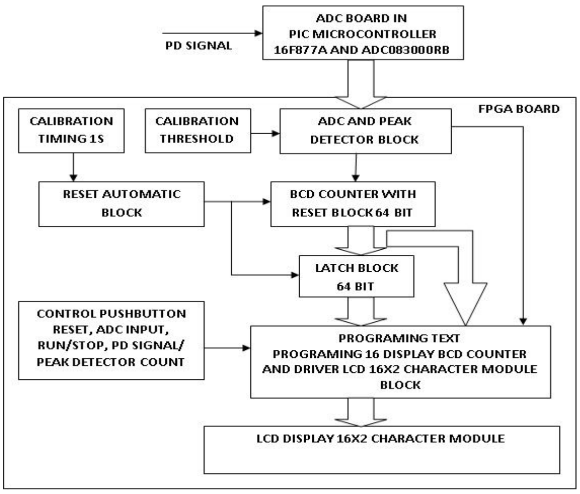


Figure 1 Block Diagram Partial Discharge Detection using Gigahertz Data Acquisition with FPGA Technology

FPGA compiler uses (Test Bench) Xilinx ISE simulator and Xilinx Synthesis Technology (XST) to process synthesis and simulate real time data from output Analogue to Digital Converter (ADC) Block to Peak Detection Block, and then process counting PD signal in Impulse Counter with Reset Block (30 bit). The impulse PD signals at the input data have very fast rise time in the range of 1 ns to 2 ns. Figure1 shows the typical block diagram for detecting and monitoring partial discharge signal.

A Partial Discharge (PD) is a flow of electrons and ions which occurs in a gas over a small volume of the total insulation system. This short duration series of events or impulse emit acoustic, optical, electrical and electromagnetic energy. PDs can be detected by measuring any of this radiation energy.[1]

The PD detection system is an automatic system that can detect and display PD signals from underground cable for easy readout. This system can work without oscilloscope, computer or any other associated costly measuring equipment. The PD signal is detected by using a highly sensitive magnetic probe. One advantage of the detection system is that it can detect the PD signal in underground cable from above the ground without outage.

The work in this paper primarily involved modeling, which comprises a FPGA compiler ISE Xilinx Synthesize Technology (XST) and ISE Xilinx simulator approach whereby the impulse signals will be processed, detected and counted using ADC with peak detector block, counter with reset block and reset automatic block. In the next stage, this method will be implemented on a lab simulation scale for testing and validation. With this method of PD detection, real

PD signals can be detected although the PD signals from magnetic probe sensor are too weak. The PD signals can also be counted and displayed clearly even if the PD signals have too much distortion. The functional approach of the ADC with peak detector block and counter with reset block will be dealt in this paper. The physics of PD generation and data acquisition system are very extensive and broad. Thus, they are not dealt in this work

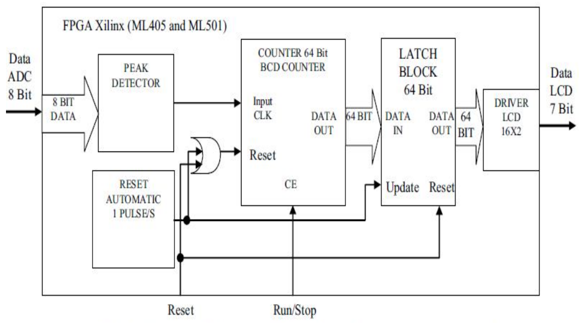


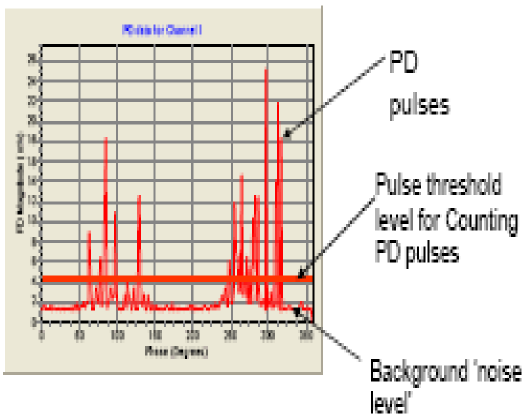
Figure 2 All Schematic Diagram of Block Diagram Complete Partial Discharge Detection Circuit using FPGA Technology

In short a PD gives rise to voltage and current pulses with time durations in the range of a few nanosecond (ns), travelling at velocity of electromagnetic waves. Due to the high sensitivity of magnetic probes, the shape of the pulse is preserved with very high integrity. [2]

II. DESIGN BLOCK OF THE PD DETECTION

Figure 2 shows the functional approach of the ADC with peak detector block, impulse counter with reset block and reset automatic block in the overall processing layout to count the PD signals. Other blocks such as latch data block and driver LCD block are not dealt in this work.[3] The detail information of each block will be described below as follows.

The reset automatic distribute the signal to BCD counter 64 bits block for reset the 64 bit BCD counter after 1 second and also distribute the signal to latch block for update data each 1 second.[4] The reset can be active manually using OR gate. The Run/Stop for 64 bit BCD Counter and Reset can be controlled by using push button from outside of FPGA board.



The function of this ADC and peak detector block is for receiving very high speed data logic from ADC module after the data is converted from analogue pulse signal and then detect the amount of peak pulse signals in logic data when processed by the peak detector in FPGA board.[5]

The process peak detector in this system is using the threshold method.[6] Figure 3 shows the simulated transient pulse and the threshold value set by the peak detector block. After finishing the processing the peak detector, the output data in this block will be sent to BCD Counter with reset block.[7]

A.1. *Block Diagram Simulation Model FPGA for ADC and*
PEAK Detection:

Figure 4 Simulation Model FPGA of ADC and PEAK Detector using VHDL Programming

Figure 4 shows the block diagram design of ADC and Peak detector block in VHDL programming when simulation model FPGA using Xilinx ISE simulator.[8]

Comparator:
(Threshold = 8F hex = 2.803 Volt)
Threshold is designed in value 2.803 Volt or 8F hex to detect PD signals in peak detector block. [9] Output of peak detector
is logic high (logic 1=5V), if the input peak detector block is more than 8F hex or if input ADC block is more than 2.803 Volt. Output of peak detector is logic low (logic 0=0V), if the input peak detector block is less than 8F hex or if input ADC block is less than 2.803 Volt.

A.2. *Design Threshold for ADC and Peak Detector Block:*

Design Threshold for Analogue Signal of Input Partial Discharge Signal:

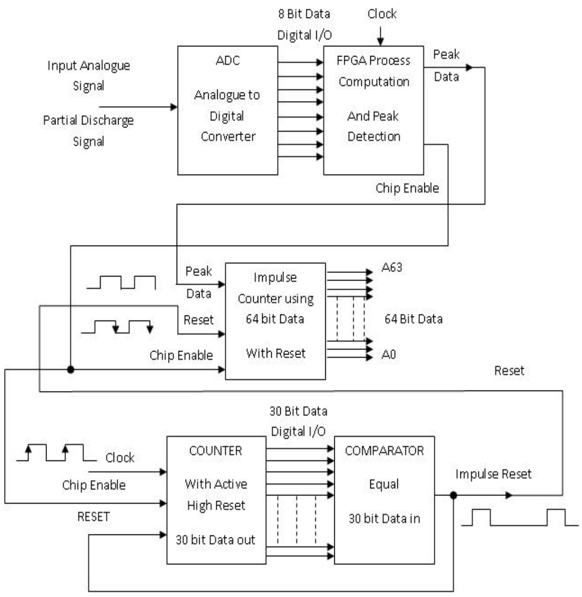


Figure 5 Block Diagram of Peak Detector, BCD Counter 64 bit, Reset Automatic Block

Figure 5 show the detail of block diagram combination of peak detector block, BCD counter 64 bit block and reset automatic block. Output BCD counter have 64 bits data logic and this output data will be sent to latch block for keep data until there is a new update data again. This paper explain detail of design each block programming and test data until output BCD Counter 64 bit data. The reset automatic block is consists of the counter 30 bits data and the comparator 30 bits data.

Figure 6 shows the design threshold and output data of peak Detector .

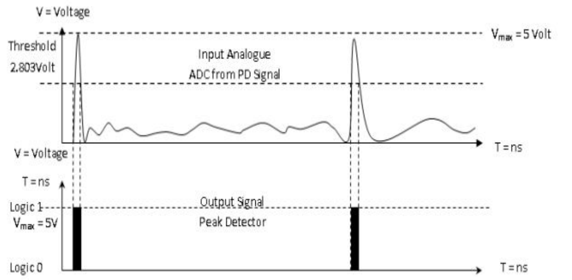


Figure6. Design Threshold and Process Peak Detection

The PD detection circuit can distinguish between PD pulse signal and harmonic signal or other noise signal because the PD detection circuit has a peak detector using threshold value, if the amplitude of signal is more than threshold value it can detect the signal and if the signal is less than threshold value it can't detect the signal. In the real system, amplitude of PD signal is always more than amplitude of noise. So it is very easy to distinguish which kind the PD signal or harmonic signal or noise signal, but the first time, the threshold value must be set between amplitude of PD signal and amplitude of Noise signal. In the system of peak detector block, the threshold value data has been set to 2.8 Volt or 8F Hex (1000 1111 bin).

Flow Chart Diagram for ADC and PEAK Detection Programming:

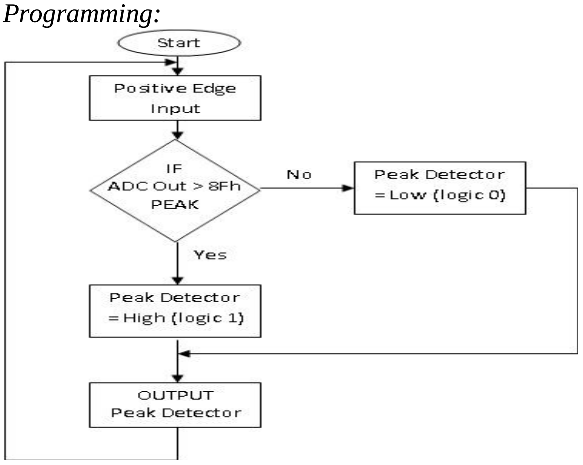


Figure7. Design Flow Chart Diagram for ADC and Peak Detection Block in FPGA Board

Figure 7 shows the design flow chart diagram for ADC and peak detector block in FPGA. Initial input is set to positive edge input.[10] The programming selects the input from ADC if the input ADC is more than 8F (threshold), the output of peak detector is high (logic1), if the input of peak detector is less than 8F (threshold), the output of peak detector is low (logic0).

Design Input Data Analogue ADC for Simulation PD signal in ADC and PEAK Detector of FPGA:

Figure 8 shows the design input PD signal to the FPGA board from the ADC board before VHDL simulation using Xilinx ISE simulator.[11]

Design input data before the simulation are as follow:
1. Input data 1st impulse from ADC is: 1110 1111 or EF hex (4.686 V).
2. Input data 2nd impulse from ADC is: 0000 0000 or 00 hex (0 V).
3. Input data 3rd impulse from ADC is: 1101 1111 or DF hex (4.372 V)
4. Input data 4th impulse from ADC is: 1011 1111 or BF hex (3.745 V)
5. Input data 5th impulse from ADC is: 0010 0000 or 20 hex (0.62 V).
6. Input data 6th impulse from ADC is: 0000 1000 or 08 hex (0.157 V).
7. Input data 7th impulse from ADC is: 0000 0010 or 02 hex (0.039 V).

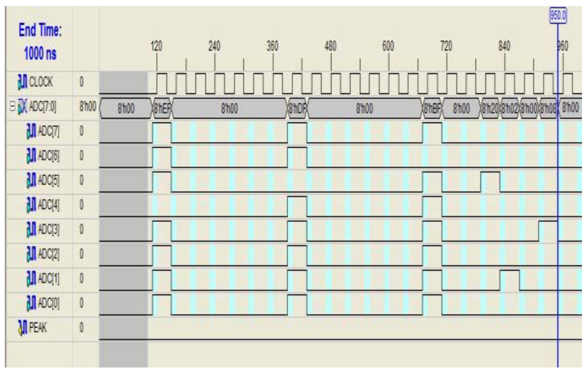


Figure8. Design Input Data Analogue PD signal for ADC and Peak Detection Block

Result of test simulation for ADC and Peak Detector Block

Programming:

Result of test in Figure 9. shows the peak detector can detect Peak of PD signal from the input signal ADC. The Peak detector in this simulation is designed to have a 2.803 V = 8F hex threshold voltage. It means that if the input signal is more than 2.803 V or 8F hex, the output of the peak detector is logic1 or 5 V and if input signal is less than 2.803 V or 8F hex, the output peak detector is logic 0 or 0 V. This ADC and PEAK Detection Block were successful run in FPGA Programming.

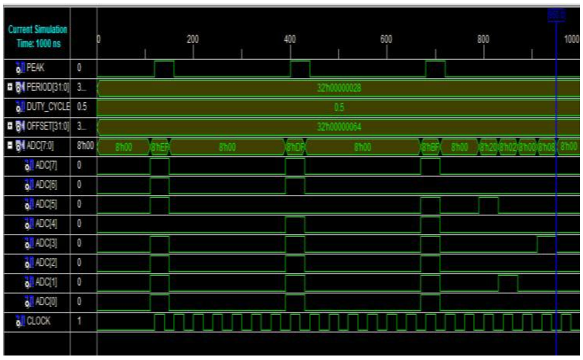


Figure 9. Simulation Model FPGA of ADC and Peak Detector Block using Test Bench Wave ISE Simulator from 0 ns until 1000 ns

Table 1. Data Result Test Peak Detector

Input Data From ADC Threshold = 8F hex = 2.803 Volt

No.	Data Binary	Data Hex	Data in Voltage	Output Peak
01.	1110 1111	EF	4.686 V	high (logic 1)
02.	0000 0000	00	0 V	low (logic 0)
03.	1101 1111	DF	4.372 V	high (logic 1)
04.	1011 1111	BF	3.745 V	high (logic 1)
05.	0010 0000	20	0.62 V	low (logic 0)
06.	0000 1000	08	0.157 V	low (logic 0)
07.	0000 0010	02	0.039 V	low (logic 0)

The experimental data from the laboratory and the VHDL programming in Table 1 shows the output peak detection is logic high when the input voltage more than 2.803 volt.

Design Counter and Reset Block:

The purpose of the Counter and Reset Block is for the counting the amount of PD signals from ADC signal and Peak detection Block in the FPGA and then perform the computation of the real time data using 64 bit digital output data in VHDL Programming. So it means the BCD counter will run as an up counter from 0 to 9,999,999,999,999,999 counting or 0000 0000 0000 0000 hex to 9999 9999 9999 9999 hex counting. The counter will return back to 0 if the reset of counter is active. In this VHDL programming, the counter is designed using reset active high (type negative edge reset) for Up Counter in FPGA. Figure 11 shows the input data analogue from ADC.

B. *Block BCD Counter with Reset*

The purpose of the BCD Counter and Reset Block is for counting the amount of PD signals from ADC signal and Peakdetection Block in the FPGA and then perform the computation of the real time data using 64 bit digital output data in VHDL Programming.

BCD Counter will return back to 0 if the reset of counter is active. In this VHDL programming, the counter is designed using reset active high (type negative edge reset) for Up Counter in the FPGA board. It means there are 16 BCD counters used in the design to detect and count the PD signal. The reset of BCD counter is controlled by the reset automatic block.

This is the flowchart of BCD counter with Reset Block:

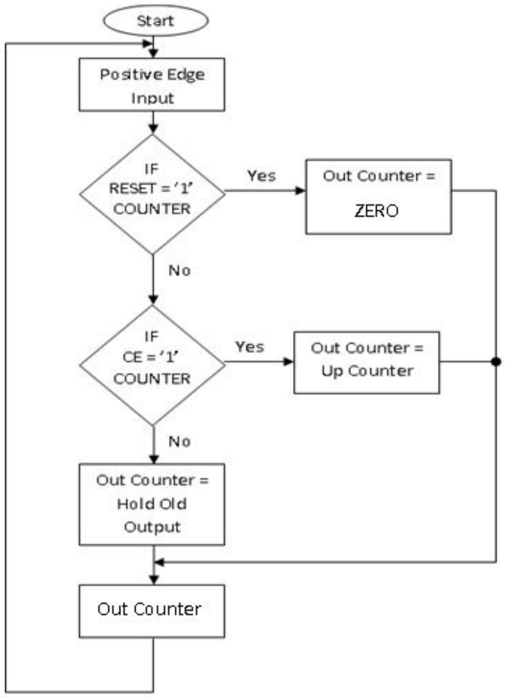


Figure 10 Design Flow Chart Diagram for Counter and Reset Block in FPGA Board

Block Diagram BCD Counter 64 bit:

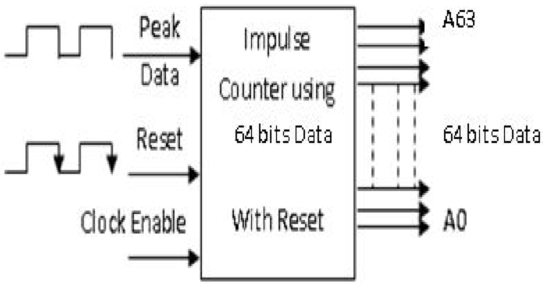


Figure 11 Block Diagram Design for 64 bit BCD Counter and Reset Block in FPGA Board

Figure 10 shows the flowchart of the 64 bit BCD counter with reset block in the FPGA board using VHDL programming. The initialization of the input is set to positive edge input. It means the BCD counter programming starts working when the clock is changed from logic 0 to 1. The data input into the BCD counter is selected by programming; if the input reset is active then the output BCD counter data is returned to zero, if the reset is not active then the program will be continued to the second selection. Here, the program will check the CE (Chip Enable); if the CE is active or logic high then the output counter will be increased by 1(up counter), but if the

CE is not active or logic low then the output of BCD counter data is not changed. Figure 11 shows the design block diagram of the 64 bit Up counter BCD with reset in the FPGA board.

Result of the Test Simulation for Counter and Reset Block Programming:

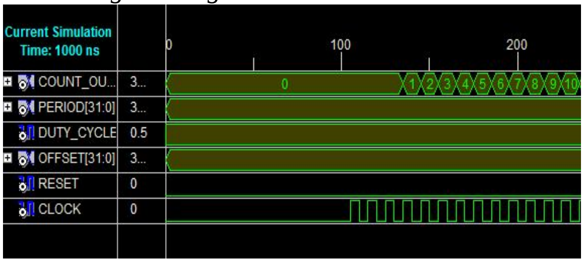


Figure12. Simulation Model FPGA of Counter and Reset Block using Test
Bench Wave ISE Simulator from 0 ns until 230 ns

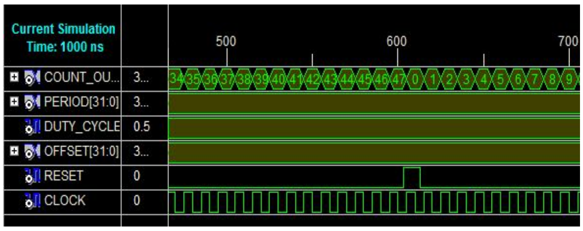


Figure13. Simulation Model FPGA of Counter and Reset Block using Test
Bench Wave ISE Simulator from 500 ns until 700 ns

Graphic Analysis:
Figures 12 and 13 shows the up counter is running from 0 to 46 hex when Reset is not active and Chip Enable is active. The running of the Up counter depends on the amount of impulse captured by Peak Detector from the input Counter and Reset Block. If the impulse reset is active in 600 ns, the counter is returned back to 0 and does the up-counting again.

C. Combination: ADC-Peak Detection, Counter-Reset Block and Reset Automatic Block

C.1. Block Diagram of ADC with Peak Detector Block, Counter with Reset Block and Reset Automatic Block

Figure 14 shows the simulation model FPGA of peak detector, up counter with reset block and reset automatic block

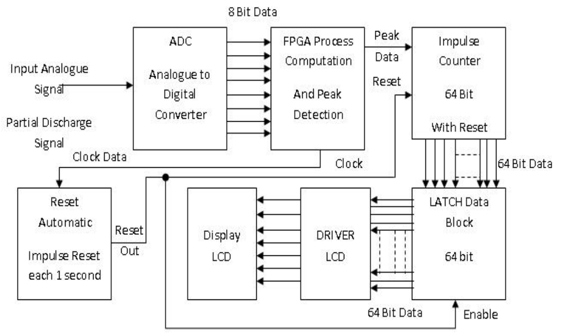


Figure14.Simulation Model FPGA of Peak Detector and Up Counter Block
using Test Bench Wave ISE Simulator

C.2. Design Peak Detector, Up Counter Block and Reset Automatic Block:
This experiment is a combination of 3 blocks programming. It is ADC and Peak Detector Block, Counter and Reset Block and Reset Automatic Blocks. The ADC and Peak detector is Working to convert data analogue signal to data digital signal and the then the data will be processed by Peak Detector Block to detect peak of PD signal from output ADC. The signal after being processed in Peak Detector Block will be counted by Counter and Reset Blocks. In the real system, the output of Counter and Reset Block will be reset and return to zero again each 1 second to determine the number of PD signals that can be detected in 1 second. The Impulse reset is generated by Reset Automatic Block. The timing of the impulse reset can be changed in the program of Reset Automatic Block. Figure 15 shows the reset automatic block in FPGA board.

C.3. Design Input Simulation for ADC with Peak Detector Block, Counter and Reset Block and Reset Automatic Block Programming:
Figure 16 shows the design of the input simulation of Combination ADC with Peak Detector Block and Counter with Reset Block in FPGA programming using Xilinx ISE simulator. Reset Block is not designed in the input simulation because of the use of the reset automatic block.

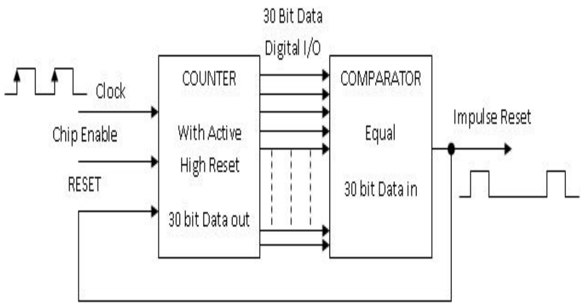


Figure15.Simulation Model FPGA of Reset Automatic Block using Test Bench

WAVE ISE SIMULATOR

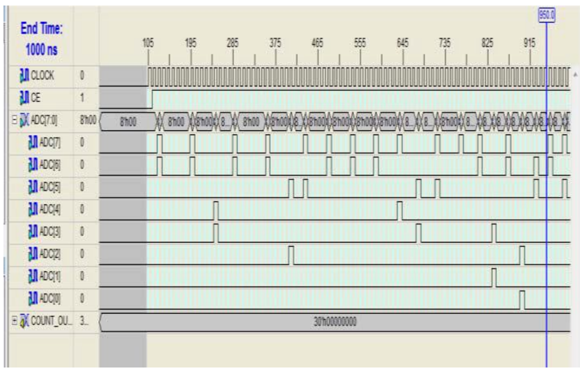


Figure 16 Design Input of Peak Detector Block, Counter Block and Reset Automatic Block.

III. SIMULATION RESULT

Figure 17 shows the simulation results of Combination ADC with Peak Detector Block, Counter with Reset Block and Reset Automatic Block in FPGA programming using Xilinx ISE simulator.

A. Result Simulation for ADC with Peak Detector Block, Counter and Reset Block and Reset Automatic Block Programming:

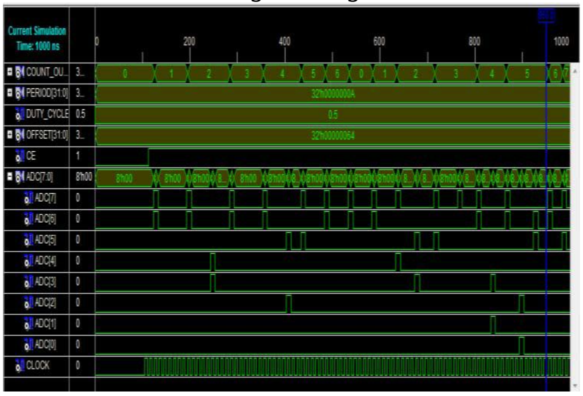


Figure 17 Result Simulation of Peak Detector Block, Counter Block and Reset Automatic Block.

B. Analysis Graphic of ADC with Peak Detector Block, Counter and Reset Block and Reset Automatic Block Programming:

The counter starts to count PD Signal when the CE (Chip Enable) is high or Active. If the data of ADC signal is more than 8Fh or 2.8 Volt then the counter will detect data and increase counting, but if the data of ADC signal is less than 8Fh or 2.8 V then the counter will not detect data and data is not update. Reset Automatic will reset to 535 ns in simulation, it is depend of timing set of Reset Automatic. In implementation the reset automatic is set to 1 second to counting how many PD signal each 1 second.

The ADC-Peak Detector and Up Counter-Reset Block and Reset Automatic block has been successful to synthesis, compile, simulate and run in FPGA Programming. Combination ADC-Peak-Counter can work successfully.

Table 2 Analysis Graphic Signal for Peak Detector and Up Counter Block in Simulation FPGA Board using Threshold 8F (2.8V)

Time	Input ADC	Peak Detector	Reset	Output Counter 64 Bit
0 ns	0	0	0	0 hex
120 ns	C0 hex	Logic 1 (high)	0	1 hex
200 ns	C0 hex	Logic 1 (high)	0	2 hex
250 ns	18 hex	0	0	2 hex
290 ns	C0 hex	Logic 1 (high)	0	3 hex
350 ns	C0 hex	Logic 1 (high)	0	4 hex
400 ns	24 hex	0	0	4 hex
430 ns	C0 hex	Logic 1 (high)	0	5 hex
480 ns	C0 hex	Logic 1 (high)	0	6 hex
535 ns	C0 hex	Logic 1 (high)	Logic 1 (high)	0 hex
580 ns	C0 hex	Logic 1 (high)	0	1 hex
630 ns	90 hex	Logic 1 (high)	0	2 hex
680 ns	28 hex	0	0	2 hex
720 ns	A0 hex	Logic 1 (high)	0	3 hex
750 ns	80 hex	0	0	3 hex
800 ns	C0 hex	Logic 1 (high)	0	4 hex
830 ns	0A hex	0	0	4 hex
860 ns	C0 hex	Logic 1 (high)	0	5 hex
900 ns	05 hex	0	0	5 hex
950 ns	C0 hex	Logic 1 (high)	0	6 hex
980 ns	A0 hex	Logic 1 (high)	0	7 hex

CONCLUSSION

The test results show that output Peak Detector can detect peak signal from the input signal ADC. The Peak Detector in this simulation is designed to have a 2.803 V = 8F hex threshold voltage. It means that if the input signal is more than 2.803 V or 8F hex, the output of the peak detector is logic 1 or 5 V and if input signal is less than 2.803 V or 8F hex, the output peak detector is logic 0 or 0 V. Combination of the peak detector block, the 64 bit BCD counter block and the reset automatic block can work successfully.

The Combination of ADC and Peak Detector Block, Counter and Reset Block, Reset Automatic Block have been successfully synthesized, compiled, simulated and run in FPGA Programming altogether. The combination of the three blocks using VHDL programming has worked successfully in FPGA Compiler.

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