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STUDY ON ESD PROTECTION CIRCUIT WITH LOW TRIGGER VOLTAGE OF DOUBLE TRIGGER STRUCTURE

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Abstract - In this paper, we propose a novel SCR-based ESD protection circuit to improve the disadvantage that it is difficult to apply to low voltage integrated circuit due to high trigger voltage of general SCR structure. The proposed structure has low trigger voltage and high robustness. Since the proposed structure has avalanche breakdown in the internal LVTSCR and SCR, the trigger occurs twice. The proposed protection circuit also has low breakdown voltage and trigger voltage by sending the current generated from LVTSCR to the SCR structure.

Keywords - ESD, SCR, LVTSCR, Trigger Voltage.

I. INTRODUCTION

With ULSI (Ultra-Scale Integration) decreased, small-sized machinery, optical and electronic products are gradually moving toward scale down. In recent years, market demand has required low power and high performance products. In order to satisfy these conditions, the semiconductor process must be considered to be capable of producing small sizes.However, miniaturized ICs are more sensitive to ESD. ESD generates high voltages and high currents, and this process takes place only during nanoseconds. ESD occurs from human body, machine and charging device. The resulting ESD / EOS problem accounts for about 35% of all IC errors [1]. To protect internal ICs from ESD failures, researchers have developed ESD protection circuits for power clamps. In theory, the ESD protection circuit for protecting the Core IC has a low trigger voltage and a high holding voltage for latch-up immunity.From the point of view, ggNMOS (gate grounded NMOS) and SCR are standard ESD protection circuits. The ggNMOS is based on a MOSFET structure and can be easily fabricated in a CMOS process. Electrical characteristics are also suitable for ESD protection with low trigger voltage and high holding voltage.However, ggNMOS has low current driving capability. Therefore, ggNMOS has a low robustness over its area, so it consumes a relatively large area of silicon than other devices to obtain high robustness [2] - [3]. On the other hand, SCR maintains high robustness due to its structural characteristics. The SCR has a current path inside the silicon substrate, which is due to the positive feedback of parasitic BJTs. In general, however, the SCR structure has a significant weakness in the latch-up effect because it has a high trigger voltage of about 20V and a low hold voltage of about 2V.Normally, increasing the holding voltage is a solution to the latch-up problem [5]. However, due to the snapback operation, the design window of the SCR is difficult to adaptively control [6].

In this paper, we propose a novel ESD protection circuit based on SCR. The trigger voltage is lowered through structural modification, and the HBM test is performed to show that the temperature characteristics are improved, which leads to high robustness. To verify the improved electrical properties, Synopsys' TCAD simulation was performed.

II. THE SCR-BASED PROTECTION CIRCUITS

2.1. LVTSCR(Low Voltage Triggered SCR)

In the case of a general SCR structure, the avalanche breakdown occurs at the junction between the N-well and the P-well, and thus has a high trigger voltage. LVTSCR has been developed to lower this trigger voltage. Figure 1 is a cross section of LVTSCR. The LVTSCR breakdown voltage is much lower than before. This is because the N + bridge region is inserted at the junction between the N-well and the P-well. This results in avalanche breakdown between the diffusion region and the well.Despite the rapid avalanche breakdown, the robustness of the LVTSCR is the same as the robustness of the SCR. Therefore, other SCR-based ESD protection circuits are mostly based on LVTSCR.

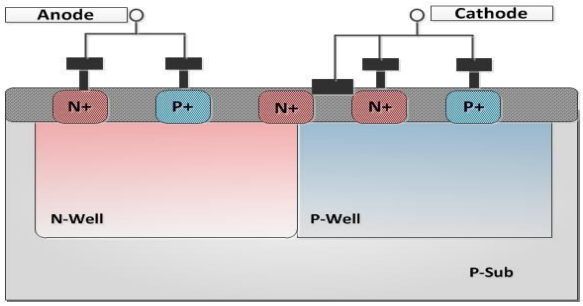

Fig.1.A cross section of LVTSCR

2.2. Proposed ESD Protection Circuit

We propose a novel SCR-based ESD protection circuit to improve the disadvantage that it is difficult to apply to low voltage integrated circuit due to high trigger voltage of general SCR structure. The

proposed structure has low trigger voltage and high robustness. The proposed ESD protection circuit is shown in Fig. There is LVTSCR on the right side and SCR structure on the left side. The SCR structure includes additional bridge N + diffusion regions and P + diffusion regions.

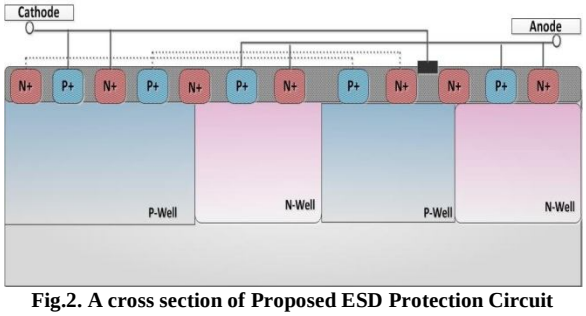

Fig.2. A cross section of Proposed ESD Protection Circuit

When the voltage of the anode terminal increases due to the ESD current flowing from the anode terminal, since the LVTSCR on the right side has a lower trigger voltage than the SCR on the left side, the potential of the N + diffusion region and the N-well of the LVTSCR rises .In the reverse biased LVTSCR, avalanche breakdown occurs when the electric field between the N + bridge region and the P-well reaches a threshold. Electron-hole pairs are generated by avalanche breakdown.The generated current is emitted from the cathode of the LVTSCR to the P + diffusion region (P + Tap) of the main SCR. The current injected into the SCR increases the potential of the P-Well of the SCR. As the trigger current increases, the potential difference between the P-well and the N + bridge of the SCR gradually decreases. This results in an avalanche breakdown between the N + bridge and the P-well. The generated electron-hole causes the parasitic NPN BJT of the SCR to turn on. The operation of the parasitic NPN bipolar operates the parasitic PNP bipolar of the SCR and the SCR is operated by the latch operation of the parasitic NPN and the PNP, so that most of the ESD current is discharged through the SCR.

III. SIMULAITON RESULTS

In this section, through the TCAD simulation, the electrical characteristics and ESD protection performance of the proposed ESD protection circuit are analyzed and the validity of the proposed protection circuit is verified by comparing with the conventional ESD protection circuit (LVTSCR).

3.1. I-V Characteristics

Fig. 3 shows the graphs of the I-V characteristics. The simulation results are verified by the Synopsys Taurus Simulation Tool. In the comparison, the proposed protection circuit has the much lower trigger voltage than the LVTSCR and slightly has the higher holding voltage.Through simulation, it can be seen that the proposed protection circuit that performs the double trigger operation provides the trigger current to the left SCR structure. In other words, it proves to obtain a low trigger voltage because it lowers the avalanche breakdown voltage between the P-Wells of the main SCR.

3.2. HBM Test

Fig. 4 is the 8kV HBM simulation results of the LVTSCR and the proposed ESD protection circuit. The simulation was conducted at the each structure of the same area. As a result, the proposed circuit, not the LVTSCR, has the better 8kV HBM robustness than others. The surface temperatures of the each protection circuit are 322K of the LVTSCR and 351K of the proposed protection circuit. The temperature is related to the robustness of the ESD standard, so the results prove the proposed circuit has the higher robustness than LVTSCR.

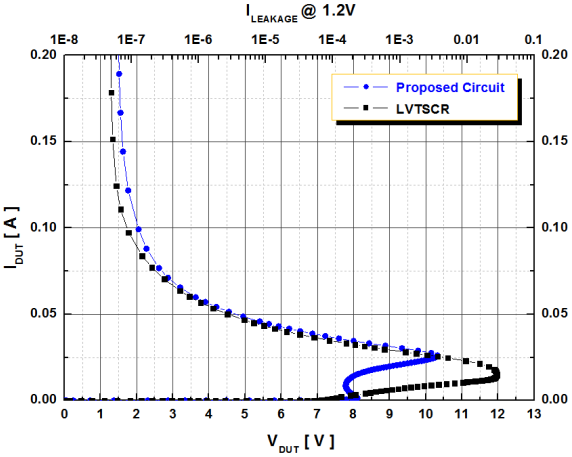

Fig.3.I-V Characteristicsof LVTSCR and the proposed ESDprotection circuit

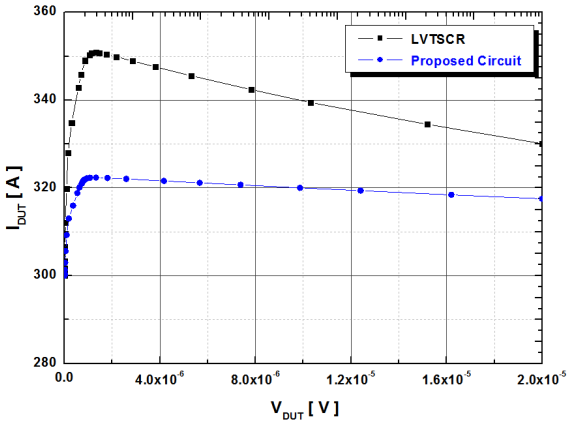

Fig.4.HBM testof LVTSCR and the proposed ESD protection circuit

CONCLUSIONS

I-V characteristics and HBM test were performed through TCAD simulation. As a result, the following two characteristics were verified.

1. The LVTSCR structure located on the right side has a reduced trigger voltage of the conventional SCR structure. By providing the trigger current to the left SCR structure, the avalanche breakdown voltage of the main SCR with the P-

well can be lowered and a lower trigger voltage can be obtained.

2. When the ESD current flows, the proposed device operates as a primary operation by LVTSCR and a secondary operation by main SCR. Due to the primary operation process by LVTSCR, the proposed device has high trigger current and low trigger current. In particular, the P + diffusion region (P + Tap) is connected to the cathode of the LVTSCR and serves to supply the trigger current from the LVTSCR to the main SCR.

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