A 16-BIT 2ND ORDER INCREMENTAL FEED-FORWARD SIGMA-DELTA MODULATOR

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Abstract—The paper presents a systematic implementation of 16-bit second order incremental FFSDM designed for DC sensor applications. The non-idealities that affect the performance of the modulator are analyzed in detail. The first stage integrator design with an op-amp gain of 90dB that is robust to the nonidealities is described. The modulator achieves a performance of 97dB SNDR with an OSR of 512 after second order (brick-wall) cascaded-integrator decimation filtering.

Keywords—Slave Delta Modulator, Switch-Capacitor Integrator, Incremental ADC.

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) are broadly classified as Nyquist-rate data converters and oversampled data converters. The former suits wideband applications with low to moderate resolution requirements (6-14 bits), whereas the later suits narrow band applications with high resolution requirements (>16 bits). In the scope of presented work, the following discussion is restricted only to oversampled data converters. Sigma-Delta ADC is an example of oversampled data converters. It makes use of frequency domain signal processing techniques to achieve high resolution (>16 bits) out of a single bit quantizer [1]. Unfortunately, the principles on which these data converters are devised make them inefficient to achieve high absolute accuracy. This limits their applicability only to communication applications and others where frequency domain metrics such as signal-to-noise-plus-distortion ratio (SNDR) and spurious-free-dynamic-range (SFDR) are of interest.

For applications such as instrumentation and measurement, the absolute accuracy is as important as the high linearity and resolution of data converter. The drawback of sigma-delta converter can be overcome by using it in incremental mode of operation [2], [3]. Incremental mode of operation establishes time domain relationship between input-output of the converter from sample-to-sample, by means of careful timing generation, to ensure high absolute accuracy.

The rest of the paper is organised as follows. Section II reviews the basic theory of sigma-delta modulators. In section III the theory of incremental operation is detailed. The architecture implemented is described in section IV. Simulation results are discussed in section IV. Finally, section V concludes the paper.

II. THEORY OF SIGMA-DELTA MODULATOR

Sigma-Delta ADC comprises of an analog sigma-delta modulator followed by a digital decimation filter known as

\[ D(z) = X(z)z^{-1} + Q(z)(1 - z^{-1}) \]  

(1)

This shows the ability of the SDM which selectively low pass filters the input signal and high pass filters.
the quantization noise of the quantizer. However, the conventional modulator topology suffers certain drawbacks as it is prone to the distortion introduced by discrete-time analog integrator in the loop. This is better understood by scrutinizing the modulator error whose z-domain representation is

\[ M_{e}(z) = X(z)(1 - z^{-1}) - Q(z)(1 - z^{-1}) \]  

(2)

It is explicit form (2) that the modulator error, which is difference signal of input and output of the modulator, contain a high pass filtered input signal. Thus, any little distortion introduced by the integrator gets boosted by high pass filtering which presents more stringent constraints on the linearity requirements of the integrator for a given resolution.

B. Feed-Forward Sigma-Delta Modulator

Feed-forward sigma-delta modulator (FFSDM) is known to be a low distortion modulator topology [4] that overcomes the short-comings of a conventional modulator. To understand how FFSDM addresses the issue consider the first-order FFSDM shown in Fig. 2. FFSDM uses an input feed forward branch that is fed to a passive capacitive adder preceding the comparator whose other input is output of the integrator. This modifies the nature of the modulator error and the output whose zdomain representation is as follows:

\[ D(z) = X(z) - Q(z)(1 - z^{-1}) \]  

(3)

\[ M_{e}(z) = -Q(z)(1 - z^{-1}) \]  

(4)

As seen in (4), the FFSDM no longer contain high pass filtered input signal in its modulator error and is more robust to integrator distortion. In fact this further relaxes the integrator swing requirements as it is now to process shaped quantization error alone. This allows designers to choose energy efficient operational amplifiers (op-amp) architectures in the integrator for required noise performance. Moreover, for higher order topologies the FFSDM obviates the need for multiple DACs in the feedback loop, unlike conventional modulator. All these features of FFSDM make it a better choice over conventional modulator.

III. INCREMENTAL MODE OPERATION OF FFSDM

The Incremental mode operation of FFSDM is intermittent in nature and differs from its free-running mode of operation. It requires all the memory elements in the modulator and digital decimator to be reset before the start of every input sample conversion. To get a deeper insight of incremental operation let us analyze the time-domain difference equation of integrator output of first-order modulator shown in Fig. 2. The integrator output is the accumulated sum of the modulator error which can be expressed on its Nth clock cycle as:

\[ y(N) = \sum_{n=0}^{N-1} (x[n] - d[n]) \]  

(5)

The reset operation of incremental mode ensure the integrator output is always bound [5] between \( \pm V_{ref} \) as shown in (6),

\[ \frac{1}{N} \sum_{n=0}^{N-1} d[n] = V_{ref} \]  

(6)

where \( V_{ref} \) is the magnitude of full scale input signal, \( \bar{x} \) is the average value of the input signal \( x[n] \).

Eq.(6) forms the basis of the incremental data conversion as it exercise a bound upon quantization error between an unknown analog input signal and digital output which is the sum of known bit stream output values of the comparator. Thus, for an \( n_{bit} \) data conversion, it requires the 1\textsuperscript{st} order modulator to be operated for \( N = 2^n_{bit} \) clock cycles, which is often referred to as over-sampling ratio (OSR), to ensure the quantization error to be less than \( \text{LSB}/2 \) (i.e. \( \text{LSB} = 2V_{ref}/2^n_{bit} \)), which is a major drawback of 1\textsuperscript{st} order incremental operation as it would require \( 2^n \) (i.e. \( 524,288 \)) clock cycles for the targeted 16-bit analog-to-digital conversion that severely limits the throughput rate of the data converter.

The incremental operation of 2\textsuperscript{nd} order FFSDM shown in Fig. 3 requires far minimum OSR compared to its 1\textsuperscript{st} order counterpart. As the output of the second integrator is the double summation of the modulator error which can be expressed on its N\textsuperscript{th} clock cycle as:

\[ y_2[N] = \sum_{m=0}^{N-1} \sum_{n=0}^{m-1} (x[n] - d[n]) \]  

(7)

whose swing can be made to be bound using incremental operation as:

\[ \left| \sum_{m=0}^{N-1} \sum_{n=0}^{m-1} d[n] \right| = V_{ref} \]  

(8)

Thus, for an \( n_{bit} \) data conversion, the OSR or the number of clock cycles (N) required for a 2\textsuperscript{nd} order FFSDM can be calculated using the following expression:

\[ (N_C)^2 = 2^n_{bit} \]  

(9)

where for the targeted 16-bit operation, it takes only an OSR of about 363 ideally. In reality the OSR required for actual circuit realization is slightly greater (i.e. 512) as we are to choose appropriate integrator gain coefficients that further alters its output swing bounds and feed forward coefficients to stabilize the modulator.
IV. ARCHITECTURE OF 2\textsuperscript{nd} ORDER FFSDM

The 2nd order FFSDM in incremental mode of operation best fit the needs of DC battery voltage sensor application for the target accuracy of 16-bits and throughput requirements of about 1ms. A fully differential discrete-time incremental second order FFSDM is shown in Fig. 4. The differential operation of the circuit implementation makes it better immune to power supply interference and other common-mode interferences. The design of the first stage integrator is very critical for the modulator performance. In fact, the most important circuit non-idealities that deter the performance of the modulator are the input referred thermal noise, finite op-amp gain and nonlinearity of the 1st stage integrator (i.e. \text{Int1}).

Despite of various noise sources in the modulator, only the input referred noise of the first stage integrator proves to be more dominant \cite{6}. As explained in the previous section, it requires modulator input, which is accompanied with input referred noise of first stage integrator, to be sampled for N clock cycles and take an average of it. Hence the noise variance or power is brought down by N times. Thus modulator can with stand OSR (N) times greater input referred noise of first stage integrator compared to its target 16-bit operation. Whereas the other noise sources of the modulator are spectrally noise shaped. Thus the modulator is tolerant to far greater noise contributions from these sources which make them non-dominant. Similarly, the modulator properties also relax the linearity requirements of the integrators as compared to target 16-bit performance, however, it is preferable to maintain the integrator linearity comparable (i.e. -98dB w.r.t. signal power). The sources of non-linearity associated with switch-capacitor integrator include non-linearity resulting from the signal dependent channel charge injection (CCI) of MOS switches and the op-amp non-linearity in itself. The CCI, if made signal independent, result in an offset which can be eliminated later on using dynamic-error-correction techniques. The parasitic-insensitive integrator topology with bottom plate sampling \cite{7} is employed for integrators. With bottomplate sampling, the switches at the virtual node (top-plate) are turned-off ahead of the switches at bottom plate. In effect, the capacitors are made to float during the disintegration of channel charge of switches at the bottom plate, which eliminates the signal dependent CCI and nonlinearity associated with them. The differential two-stage op-amp architecture with folded cascode in the first stage, followed by, common source amplifier in the second stage, is chosen for the op-amp used in the first stage integrator because of its stringent gain, linearity and output swing requirements. It is required to ensure a finite differential op-amp gain of 90dB \cite{8} for the required 16-bit operation. The common-mode-feedback (CMFB) is the key for its differential operation where a continuous-time two differential
pair CMFB and a switch-capacitor CMFB [9] are employed in the first and second state of the op-amp respectively. Whereas the second stage integrator is chosen with a single stage folded cascode op-amp due to its relaxed constraints. Both the integrators are designed for a unity-gainbandwidth of about 12MHz, which is required to ensure a settling error LSB/4 corresponding to 16-bit operation. Dynamic error correction techniques such as auto-zeroing (AZ) or chopper-stabilization (CHS) are usually required for high absolute accuracy in order to eliminate the offset errors introduced with the signal independent CCI of sample switches, input referred offset and flicker noise of the op-amp in first stage integrator. These techniques usually end up in either more on-chip area or added complexity as AZ requires additional capacitors to sample the offset and CHS requires additional switches and a slower clock frequency. To avoid these drawbacks system chopping is chosen at expense of half the actual throughput rate. It requires ADC to resolve the input twice with swapped modulator input polarity and take a difference average to eliminate the offset.

V. SIMULATION RESULTS

The second order FFSDM is implemented in Cadence environment using AMS C35 technology on a 3.3V power supply. The incremental FFSDM is made to operate with a sample frequency of 1MHz, to meet the ADC bandwidth requirements of about 975Hz, as simulations mandate an OSR of 512 for 16-bit incremental operation. In sigma-delta mode of operation, the modulator is made to operate free running without reset. Spectral analysis of the modulator is carried out with an FFT of 214 (i.e. 16384) points using transient simulations without transient noise enabled as shown in Fig. 5. It achieved an in-band SNDR of about 104.3dB. These simulations substantiate that non-linearity, finite op-amp gain and settling error of the first stage integrator are not limiting the modulator performance. However, the modulator performance is limited to an inband SNDR of 98.2dB with transient noise enabled in the simulations as shown in Fig. 6. It substantiates the fact that the thermal noise of the first stage integrator is the major bottleneck for performance of all the non-idealities. In incremental operation, to evaluate the performance of the modulator alone an ideal (brick-wall) second order cascaded integrator decimation filter is implemented using a VerilogA behavioural model in cadence. The spectral analysis of the decimation filter is carried out with a 256 point FFT as shown in Fig.7. It achieved an SNDR of 97.6dB which corresponds to an ENOB of about 16-bits which is the targeted performance.

CONCLUSION

In this paper, a circuit implementation of second-order incremental feed-forward sigma-delta modulator is presented in detail. The thermal noise of the first stage integrator is identified as the major bottleneck for the modulator performance. The modulator achieved a performance of 97dB SNDR after ideal second order cascaded integrator decimation filtering.

REFERENCES

A 16-Bit 2nd Order Incremental Feed-Forward Sigma-Delta Modulator