A NOVEL APPROACH FOR LEAKAGE POWER REDUCTION TECHNIQUES IN CMOS VLSI CIRCUITS

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Abstract— CMOS technology is the key element in the development of VLSI systems because CMOS circuits consume very little power. Leakage power dissipation has become an overriding concern in nanometer CMOS technologies. International Technology Roadmap for Semiconductors (ITRS) reports that leakage power dissipation may come to dominate total power consumption. A comprehensive study and analysis of various leakage power minimization techniques like Base Case, Forced Stack, Sleep Transistor and Sleepy Stack etc. have been proposed in this paper. In this paper new methods have been proposed for leakage power reduction in 45 nm technology. The performance parameters of proposed methods are compared with the previous standard leakage reduction techniques using microwind software and reported in this paper.

Index Terms— Leakage power, Sub-threshold leakage power, Sleep transistor, Variable body biasing.

I. INTRODUCTION

Leakage power consumption is one of the major concerns in CMOS VLSI circuits. Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub threshold current exponentially increasing with decreasing device dimensions. To overcome the power dissipation problem many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid trade-offs between power, delay and area. Thus designers are required to choose appropriate techniques that satisfy application and product needs. The power dissipation of a logic gate is given by,

\[ P = 0.5aC \cdot V^2f + V \cdot (I_L + I_s + I_d) \]

Where, \( P \) = Power dissipation, \( a \) = Average no. of logic transitions in a given cycle, \( C_L \) = Load capacitance of the circuits, \( V \) = Supply voltage, \( f \) = Frequency operation, \( I_L \) = Source current, \( I_s \) = Gate current, \( I_d \) = Drain current.

Power dissipation of CMOS consists of dynamic and static components. Dynamic power dissipation, resulting from continuous transistors’ switching, charging and discharging of capacitances contributed the most to the total chip’s power dissipation in CMOS circuits thus most efforts were devoted towards reducing it. But as technology advances, leakage power dissipation increases in a much faster rate than dynamic power. Leakage power is static power dissipation and can be described as the power that is dissipated through transistors without producing any useful outcome. For example, if the gate voltage of a transistor is lower than the threshold voltage (required voltage to turn ON the transistor), the transistor is not completely OFF and a small current still flows which is known as sub threshold leakage current. Since leakage power dissipation is approaching 40% of today’s high performance microprocessors total power dissipation, new techniques and new technology innovations are urgently needed to reduce leakage current components.

According to ITRS reports gate leakage current will reach unacceptable levels (especially in portable devices) and will mandate the introduction of new high dielectric (High-K) materials for low power and high performance applications. Leakage current is the current that flows through a transistor when it is switched off. It depends on gate length, oxide thickness and varies exponentially with threshold voltage, temperature and other parameters. To reduce leakage power, a novel approach has been proposed in this paper, which provides a new choice to the low leakage power VLSI designers. Previous techniques are summarized and compared with proposed approach presented in this paper.

II. LEAKAGE POWER

Figure 1 shows that sub threshold leakage current (power) is becoming the primary source of power dissipation in CMOS below 90 nm technology. Sub-threshold leakage current is very significant component of the leakage power and this current passes from drain to source through the channel [1-2]. The sub-threshold leakage current is caused basically due to carrier diffusion between the source and drain region of the transistor in weak inversion.

Fig. 1: Process technology vs. Dynamic & Leakage power
In this section, we discuss about the previous low-power techniques that primarily target reducing leakage power consumption of CMOS circuits. Technology scaling is one of the driving forces behind the tremendous improvement in performance, functionality and power in integrated circuits over the past several years. Power dissipation has become a very critical design criterion with miniaturization and the growing trend towards wireless communications. For deep-submicron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced which in turn reduces the dynamic power dissipation to an extent. However, the sub threshold leakage current increases exponentially thereby increasing static power dissipation [3]. Modern digital circuits consist of logic gates implemented in the CMOS technology. Power consumption has two components: Dynamic Power and Leakage power [4]. The dynamic power is consumed only when the circuit performs a function and signals change. Leakage or static power is consumed all the time i.e. even when the circuit is idle. It is unnecessary and one would like to eliminate it [5]. Scaling down of the technology has led to increase in leakage current. The efficient methodologies have been proposed for reducing leakage current in VLSI design [6].

Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18-µm technology and above) the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling focused on dynamic power reduction. However, as the feature size shrinks e.g. 0.09 µm and 0.065 µm, static power has become a great challenge for current and future technologies based on the ITRS reports [7]. A novel ultra-low leakage CMOS circuit structure called sleepy stack, can retain logic state during sleep mode while achieving ultra-low leakage power consumption. Although the sleepy stack incurs some delay and area overhead. The sleepy stack technique achieves the sub threshold leakage power consumption can be nearly equal to dynamic power consumption [8].

Several techniques at circuit level and process level are used to efficiently minimize leakage current which lead to minimize the power loss and prolong the battery life in idle mode. A novel approach, named “Zigzag with keeper” was proposed at circuit level for the reduction of power dissipation [9]. Sub-threshold leakage power is compatible to dynamic power consumption, thus handling leakage power is a great challenge. A new circuit structure named “stacking with sleepy keeper Approach” has been proposed to tackle the leakage problem [10].

III. LEAKAGE POWER REDUCTION TECHNIQUES

Leakage current is a primary concern for low-power, high-performance digital CMOS circuits. The exponential increase in the leakage component of the total chip power can be attributed to threshold voltage scaling. Numerous design techniques have been proposed to reduce standby leakage in digital circuits. In all the approach, transistor are placed between two parallel rows continuous $V_{dd}$ and $V_{ss}$ ($G_{nd}$). Here we review previously proposed circuit level approaches for sub threshold leakage power reduction.

a) Base Approach: The base approach circuit contains only the PMOS and NMOS network. It is a state saving technique and has a minimum area requirement for implementation.

b) Forced Stack Approach: This approach forces a stack effect by breaking down an existing transistor into two half size transistors [11]. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach. The forced stack approach can achieve huge leakage power saving while retaining the logic state and it does not use the high threshold voltage ($V_{th}$) of transistor.

c) Sleep Transistor Approach: A sleep PMOS transistor is placed between power supply ($V_{dd}$) and the pull up network. Similarly sleep NMOS transistor is placed between ground ($V_{ss}$) and pull down network. Sleep transistors turn off the circuit by cutting off the power rails in idle mode thus can reduce leakage power effectively. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. So the technique results in destruction of state. Usually, high threshold voltage is used for sleep transistor.

d) Sleepy Stack Approach: Sleepy stack approach can be developed by combination of sleep and stack approach [12]. This technique divides existing transistors into two half size transistors like the stack approach. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current in state saving mode. Subsequently delay is decreased during active mode. Thus by combining two techniques, we can achieve (i) ultra-low power leakage and (ii) retention of state. The main drawback of the sleepy stack technique is that it increases area a lot.

IV. PROPOSED LEAKAGE POWER MODELS

In this section, the new leakage power reduction techniques have been introduced. The proposed circuit is compared with well-known previous approaches such as Base Case, Forced Stack, Sleep Transistor and Sleepy Stack etc.
A. Sleep Transistor Approach with NMOS:
The operation of proposed sleep transistor approach with NMOS technique is discussed in this section. Figure 2 shows sleep transistor approach with NMOS structure.

In this proposed technique, PMOS and NMOS sleep transistors are used for leakage power reduction and an extra NMOS is added because of sleep transistor technique is a state destructive technique. To retain the state, NMOS is used in this proposed method. Sleep transistors have high threshold voltage i.e. multi-threshold technique is used here. Transistor stacking technique is also involved in this method for the purpose of reducing leakage current during active mode or run time. Sleep transistors reduce leakage current during idle mode.

B. Forced NMOS Transistor Inverter:
In forced NMOS inverter if input is given low as compared to threshold voltage, then at the same time PMOS turns on and NMOS turns off and if input is given high at the gate terminal as compared to threshold voltage, then at the same time PMOS turns off and NMOS turn on. Here, the two NMOS transistors increases the delay in the flow of current, which ultimately decreases the leakage power in the circuit. Figure 3 shows forced NMOS transistor inverter structure.

C. Variable Body Biasing With Bypass:
Variable body biasing technique is used for the leakage power reduction. The proposed technique Variable body biasing with bypass is shown in Fig. 4. Here the source of the PMOS sleep transistor is connected to the body of other PMOS sleep transistor for having so called body biasing effect. Similarly for the NMOS sleep transistor, variable body biasing is increasing the threshold voltage for the purpose of reducing the leakage power because increase in threshold voltage results decrease in leakage current. As mentioned above, sleep transistor technique is combined with variable body biasing technique. The sleep transistor is a state destructive technique, to get the exact state at output; bypass has been included in this method. Bypass is used for retaining the state at the output.

V. METHODOLOGY
In this section we describe the experimental method. First we describe how to make a schematic diagram and create a layout diagram by using the tools. Secondly, we describe how to obtain the results in term of power dissipation, delay, current and area. Experimental Methodology: Two type of window are involved in this tool. Schematic called DSCH and MICROWIND where layouts are design. Schematic and layout are designed for all type of approach. Schematics are used to make different type of digital and analogue circuit and all the parameter are estimated with the help of microwind window where the layout are design.

These parameter are power dissipation, delay, current and area at different technology of all considering approach. Here Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in microwind software. After the compilation of Verilog file, the layout for the circuit diagram has drawn in schematic and it will be generated in microwind software. After that simulations are performed on the layout generated.
using Verilog files. All the simulations are carried down at the room temperature of 270°C.

VI. SIMULATIONS AND EXPERIMENTAL RESULTS

In this section, all proposed models are simulated using microwind software in 45 nm technology and the results are depicted in Fig.6 to Fig.8 for measurement of power consumption, delay, current and layout area for the design approaches i.e. base approach, sleep transistor approach with NMOS, forced NMOS transistor inverter and variable body biasing with bypass approach etc.

The corresponding schematic diagram and simulations of sleep transistor approach with NMOS are shown in Fig. 6(a) to Fig. 6(c). From Fig. 6(a) the layout area is measured. Figure 6(b) is used to measure the power and time delay and from Fig. 6(c) the current is measured. It can be observed from the waveforms that the performance of the sleep transistor approach with NMOS is very good as compared to the conventional sleep transistor approach. In this case delay is also less, however maximum current in the proposed approach is more.

The simulation results of forced NMOS transistor inverter are shown in Fig. 7(a) to Fig. 7(c). The layout area is measured from Fig. 7(a) and the power and time delay are measured from Fig. 7(b). Figure 7(c) is used to measure the current. It is concluded from figures that the time delay increases and leakage power consumption becomes low. This technique has much better performance and deliver more current.

The corresponding schematic diagram and simulations of variable body biasing with bypass approach are shown in Fig. 8(a) to Fig. 8(c). From Fig. 8(a) the layout area is measured. Figure 8(b) is used to measure the power and time delay and from Fig. 8(c) the current is measured. It can be observed from the waveforms that the performance of the variable body biasing with bypass approach is very good as compared to the conventional sleep transistor approach. In this case delay is also less, however maximum current in the proposed approach is more.
The corresponding schematic diagram and simulations of variable body biasing with bypass technique are shown in Fig. 8(a) to Fig. 8(c). Figure 8(a) is used to measure the layout area and the power and time delay is measured from Fig. 8(b). Figure 8(c) is used to measure the current. It can be observed from the waveform that the performance obtained from the variable body biasing with bypass is very good. This approach has less time delay and deliver maximum current as compare to base case and conventional techniques. This technique reduced maximum leakage power as shown in figures.

Simulation results of the proposed leakage power reduction techniques are compared with well-known previous leakage power reduction techniques in terms of power, delay, current and area as given in the table 1. It can be observed from the comparison tables that there is a considerable reduction in power, delay, current and area in the proposed method as compare to base case i.e. inverter and conventional techniques.

Table 1 Comparison table between previous and proposed leakage power reduction techniques.

<table>
<thead>
<tr>
<th>Technique</th>
<th>Power (μW)</th>
<th>Delay (ns)</th>
<th>Current (mA)</th>
<th>Area (μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base approach</td>
<td>11.176</td>
<td>9</td>
<td>0.286</td>
<td>13.86</td>
</tr>
<tr>
<td>Forced Steeck</td>
<td>8.876</td>
<td>20</td>
<td>0.097</td>
<td>28.50</td>
</tr>
<tr>
<td>Sleepy Transistor</td>
<td>2.747</td>
<td>4.5</td>
<td>0.096</td>
<td>33.06</td>
</tr>
<tr>
<td>Sleepy Stock</td>
<td>6.014</td>
<td>9</td>
<td>0.130</td>
<td>50.22</td>
</tr>
<tr>
<td>Sleepy Transistor Approach with NMOS</td>
<td>3.774</td>
<td>0.199</td>
<td>0.140</td>
<td>0.4224</td>
</tr>
<tr>
<td>Forced NMOS Transistor Inverter</td>
<td>4.046</td>
<td>0.220</td>
<td>0.069</td>
<td>0.0424</td>
</tr>
<tr>
<td>Variable Body Biasing With Bypass</td>
<td>1.317</td>
<td>1.600</td>
<td>0.274</td>
<td>0.5376</td>
</tr>
</tbody>
</table>

CONCLUSION

In nanometer scale CMOS technology, sub threshold leakage power is compatible to dynamic power consumption and thus handling leakage power is a great challenge. Leakage power is a primary concern for low-power, high-performance digital CMOS circuits. In this paper an efficient methodology has been reported to tackle the leakage problem of CMOS circuits. The simulation results of proposed methods shows ultra-low static power consumption with state saving. The proposed variable body biasing with bypass is more power efficient compared to other methods.

REFERENCES