SIMULATION OF NANOSCALE DUAL-MATERIAL GATE DOUBLE-LAYER GATE- STACK BULK PLANAR JUNCTIONLESS TRANSISTOR

NEHA U. CHAUDHARI, S. C. WAGAJ, SNEHAL R. MULMANE

1,2,3Electronics Engineering, JSPMs Rajashri Shalu College of Engineering, Tathawade, Pune, India. 
E-mail: 1nehachaudhari88@gmail.com, 2snehmulmane@gmail.com, 3scwagaj@yahoo.com

Abstract— A simulation study of analog and digital parameters of dual material gate bulk planar junctionless transistor are discussed. The characteristics are demonstrated and compared with DMG BPJLT and Single Material (conventional) Gate (SMG) BPJLT. The DMG BPJLT presents superior Subthreshold Swing (SS) and reduces Drain Induced Barrier Lowering (DIBL) as compared with SMG BPJLT. By adjusting the metal work functions; channel potential and electric field distribution along the channel can be controlled.

Keywords— Bulk Planer Junctionless Transistor (BPJLT), junctionless transistor (JLT), Short Channel Effects (SCE). Dual material Date Bulk Planer Junctionless Transistor (DMG-BPJLT), single Material Gate (SMG)

I. INTRODUCTION

Transistors are the basic building block of all modern electronic devices. A conventional structure of all transistors contains p-n junctions in source-channel and drain-channel region, p-n junction is formed by making contact of doped semiconductor with trivalent impurity in one side and pentavalent impurity on the other side. Depending on the bias applied to gate terminal channel allow or block current flow, for example when positive bias is applied to gate terminal of n-channel MOSFET, an electric field developed across gate dielectric tends to attract electrons from substrate to channel region and creates inversion layer helps drain to source current flow. The size of electronics instruments reduces as technology improves, according to Moore’s law, transistor dimensions have been shrinking 30% every 3 years. Moore’s law only describes the rate of increase in transistor density, by reducing the physical device dimension of transistor both circuit speed and physical device dimension of transistor both circuit speed and packaging density will improves this technique is called as scaling. There are some drawback of scaling when reaches to 20nm regime, scale transistors have some undesirable characteristics namely Drain Induced Barrier Lowering(DIBL), Sub-threshold Swing(SS), Velocity Saturation, Gate Induced Drain Leakage(GIDL), Gate oxide leakage etc. all effects are collectively called short channel effects (SCE). Number of research group work to overcome this drawback with different attributes like structural change, material change etc. BPJLT(Bulk Planer Junctionless Transistor) which is a source-drain junction free transistor accompanied with a junction isolation. It is thus junctionless in the source-channel-drain path but needs a junction in the vertical direction for isolation purposes. DMG BPJLT with high k spacer and gate stack offers simultaneous improvement of subthreshold swing, threshold voltage, Ion/Ioff ratio as well as reduces Drain Induced Barrier Lowering(DIBL). Thus the characteristics gets improved. It offers simultaneous improvement of Short Channel Effects (SCE) as well as transconductance.

II. DETAILS EXPERIMENTAL

2.1 BPJLT(Bulk Planer Junctionless Transistor)

BPJLT(Bulk Planer Junctionless Transistor) which is a junction free transistor accompanied with a junction isolation. It is thus junctionless in the source-drain path but needs a junction in the vertical direction for isolation purposes. Junctionless transistor (JLT), which does not have p-n junction in the source–channel-drain, the advantages of the BPJLT over the existing JLT versions are as follows:

1. Simple process flow
2. Flexibility in gate material
3. Better performance against SCE
4. Low thermal budget
5. More Scalable

![Fig.1.- Schematic representation of BPJLT](image-url)

Here SiO2 is used as a Gate oxide and Source(S), Drain(D) are made up of Aluminium material. Doping concentration of channel is 1xe^18 and for substrate doping concentration is 5x15. For channel, doping is donor type and for substrate, doping is acceptor type. In the BPJLT, when zero gate bias is applied, the device layer is depleted from both top and bottom because of its workfunction difference.
with the gate electrode on one side and the oppositely doped substrate on the other. portion of the physical device layer that is depleted by the gate at zero bias is the “Effective Device Layer”. As a positive bias is applied to the gate, this effective device layer comes out of depletion and results in a conducting channel between the source and the drain.

2.2 Dual Material Gate BPJLT

Normally we use the single gate material in bulk planar junctionless transistor. But to improve the characteristics this paper used dual gate material with spacer and gate stack. The aim of this paper is to reduce the short channel effects and improved carrier transport efficiency. A DMG JLT has two gate material;M1 and M2, with different workfunctions, denoted by WM1 and WM2 respectively. Workfunction of M1 (WM1) is greater than of workfunction of M2 (WM2). Here WM1 is 5.2 and WM2 is 4.77.

In this paper dual material gate BPJLT is simulated for different gate length varying from 20 nm to 50 nm. Doping concentration is same as that of SMG BPJLT. A thin passivating layer of SIO2 between bulk and high-K dielectric, so as to form a gate-dielectric stack, is a good approach to balance between the advantages and limitation to high-K /Si system. Introducing a high-K spacer with Ksp of air (1) on either sides of the gate can enhance the fringing electric fields through the spacer and deplete the device layer beyond the gate edges in the OFF-state. This would result in an effective increase in the length of depleted silicon region (effective channel length) and hence improve subthreshold characteristics. However, in the ON-state having zero electric field can leave the ON-state current unaffected with the use of high-K spacer.

Table 1. Parameters of BPJLT

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical gate length (Lg)</td>
<td>20-50 nm (Variable)</td>
</tr>
<tr>
<td>Channel thickness</td>
<td>10 nm</td>
</tr>
<tr>
<td>Channel doping (Nd)</td>
<td>1e15 cm$^{-3}$</td>
</tr>
<tr>
<td>Gate Oxide Thickness (Tox)</td>
<td>SiO2 1nm</td>
</tr>
<tr>
<td>Substrate doping (Nw)</td>
<td>5e15 cm$^{-3}$</td>
</tr>
</tbody>
</table>

Any increase in gate voltage beyond the flatband wold drive the channel into accumulation, and this can be further enhanced by the presence of high-K spacers to augment the drain current.

III. RESULT AND DISCUSSION

Ion / Off ratio is increased for DMG-BPJLT than SMG-BPJLT.

It was observed that the use of a high-k dielectric and air as a spacer brings an improvement in the OFF-state current by more than one order of magnitude, thereby making the device more scalable. However, the on-state current marginally decreases and off-state current by more than one order of magnitude, thereby making the device more scalable.

Table 1. Table of Ion/Ioff ratio for different Gate length

<table>
<thead>
<tr>
<th>Gate Length (nm)</th>
<th>Ion(Ioff=50nmv, $V_{GS}=1$V)</th>
<th>Ioff(Ion=50nmv, $V_{GS}=0$V)</th>
<th>Ion/Ioff Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>6.8×10$^{-5}$</td>
<td>3.43×10$^{-8}$</td>
<td>1.98×10$^{2}$</td>
</tr>
<tr>
<td>30</td>
<td>5.9×10$^{-5}$</td>
<td>1.09×10$^{-9}$</td>
<td>5.41×10$^{4}$</td>
</tr>
<tr>
<td>40</td>
<td>5.1×10$^{-5}$</td>
<td>5.32×10$^{-11}$</td>
<td>9.5×10$^{6}$</td>
</tr>
<tr>
<td>50</td>
<td>3.5×10$^{-5}$</td>
<td>8.39×10$^{-13}$</td>
<td>0.4×10$^{8}$</td>
</tr>
</tbody>
</table>

However, the ON-state current is only marginally affected by increasing dielectric constant of spacer. The effects of spacers width (Wsp) on device performance were also studied.

The ON-state current marginally decreases and OFF-state current marginally increases with increase in spacer width.

Table 1. Table of comparison of Ion/Ioff ratio for SMGBPJLT and DMGBPJLT.

<table>
<thead>
<tr>
<th>Device</th>
<th>Ion(A) [Vdd=1V, $V_{GS}=1$V]</th>
<th>Ioff(A) [Vdd=1V, $V_{GS}=0$]</th>
<th>Ion/Ioff Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMGBPJLT</td>
<td>1.126 ×10$^{8}$</td>
<td>8.822 ×10$^{6}$</td>
<td>1.276 ×10$^{2}$</td>
</tr>
<tr>
<td>DMGBPJLT</td>
<td>9.653 ×10$^{8}$</td>
<td>5.150 ×10$^{6}$</td>
<td>1.874 ×10$^{2}$</td>
</tr>
</tbody>
</table>

In this paper, a 2-D Simulation of a novel device called Bulk Planar Junctionless transistor (BPJLT) is...
Simulation of Nanoscale Dual-Material Gate Double-Layer Gate-Stack Bulk Planar Junctionless Transistor

carried out, to improve the figure of merits. For this VISUAL TCAD Simulator is used. It helps to overcome various challenges of scale transistors, to study this simulation of conventional MOSFET’s and JLT carried out. Further, simulation of BPJLT and Dual Material Gate BPJLT is carried according to literature review to study properties and find superior among them. Furthermore, high-k dielectric (SiO₂, Si₃N₄, HfO₂) is choose as gate oxide to study the input-output characteristics. Out of different combinations of gate oxide/spacer dielectric material considered namely, SiO₂, Al₂O₃ and HfO₂: SiO₂ as a gate oxide and HfO₂ as high-K dielectric offer highest Ion/Ioff ratio.

To prevent direct gate tunneling in very thin oxides, replacement if SiO₂ gate dielectric by alternatives materials with higher permittivity is envisaged. However, introduction of this high-K dielectrics comes with its own set of problems. A thin interfacial SiO₂ passivating layer helps circumvent the disadvantage. Thus, high-K/SiO₂ system is studied for its impact on the performance of BPJLTs, with or without the DMG electrode. Combining the advantages of JLT, DMG, and high-K spacer dielectric, we can propose dual-material gate along with high-K spacer dielectric(DMG-SP)BPJLT.

Drain Induced Barrier Lowering (DIBL) reduces as gate length increases and results of DMG BPJLT are improved than SMG BPJLT. Subthreshold Swing is defined as the variation in the gate voltage required to have a decade variation in drain current. For a BPJLT, Subthreshold Swing is given by the following equation.

\[
SS(m\text{V}) = \frac{kT}{q}\ln(10)\left(1 + \frac{C_d}{C_{ox}}\right)
\]

Where \(T\) is the temperature in degrees Kelvin, \(q\) is the charge of electron, \(C_d\) is the depletion Capacitance, \(C_{ox}\) is the gate oxide capacitance.

Subthreshold Swing decreases as gate length increases and results of DMG BPJLT are improved than SMG BPJLT.

**CONCLUSION**

DMG BPJLT gives higher subthreshold swing and improved carrier transport efficiency, transconductance and reduces the drain induced barrier lowering thereby improving analog performance of the device. High-K gate stack material helps to reduces SCE and improve device performance.
REFERENCES


**Simulation of Nanoscale Dual-Material Gate Double-Layer Gate-Stack Bulk Planar Junctionless Transistor**