REDUCTION OF FAR END CROSSTALK ON HIGH SPEED PRINTED CIRCUIT BOARD USING SINUSOIDAL MICROSTRIP LINES

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Abstract - In the recent electronic era, the reliability of circuits on printed circuit boards (PCBs) is affected by severe noise which is caused by high speed and low voltage operation as well as layout constrains compounded by limited space and high circuit density. The sinusoidal microstrip lines are proposed to eliminate far-end crosstalk in parallel high speed interfaces. By this modification increase in capacitive coupling ratio is obtained and is made equal to inductive coupling ratio. Mitigation of far-end crosstalk, near-end crosstalk, return loss and insertion loss were achieved on an FR4 printed circuit board by adjusting unit section of length. The far-end crosstalk and the near-end crosstalk has been observed to be reduced by 16% and 21% respectively than the conventional methods used. The added objective of reducing the return loss and insertion loss was also reduced by 57% and 22% respectively.

Keywords - Microstrip line, signal integrity, NEXT, FEXT, jitter.

I. INTRODUCTION

In this advanced period of modern communication the rise of digital electronics is such that the binary values have to be transmitted with low bit rate, high speed and fidelity. By implementing these aspects, the signal gets degraded and the device fails. Microstrip line, which is a category of transmission line are widely implemented for high speed signal interface on PCBs[3]. In parallel microstrip lines for SATA interconnect[7], electromagnetic coupling generates far-end crosstalk (FEXT) Eqn(1) and near-end crosstalk (NEXT) Eqn(2).

\[
V_{FEXT}(t) = \frac{1}{2}\left[\frac{C_m}{C_T} - \frac{L_m}{L_s}\right] T_p \frac{dV_a(t-T_p)}{dt} \tag{1}
\]

\[
V_{NEXT}(t) = \frac{1}{4}\left[\frac{C_m}{C_T} + \frac{L_m}{L_s}\right] V_{in}(t) - V_{in}(t-2t_f) \tag{2}
\]

Where \(t\) is time, \(C_m\) is mutual capacitance, \(C_T\) is the sum of mutual capacitance and self capacitance of the microstrip line, \(L_m\) is the mutual inductance, \(L_s\) is the self inductance of a microstrip line, \(C_m/C_T\) is the capacitive coupling ratio, \(L_m/L_s\) is the inductive coupling ratio, \(T_p\) is the propagation time through the transmission time, \(t_f\) is the flight time and \(V_{in}(t)\) is the voltage applied to the aggressor line. The far-end crosstalk voltage comprises of a negative pulse at the rising edge of the applied input, hence inductive coupling ratio is greater than the capacitive coupling ratio in microstrip line with one side exposed to air. As shown in Eqn(1), Eqn(2) both \(V_{FEXT}\) and \(V_{NEXT}\) can be reduced, if \(C_m/C_T\) is increased to equal \(L_m/L_s\). A traditional methodology of reducing FEXT and NEXT of two parallel microstrip lines is to widen the space between them Fig1.(a). This reduces both the coupling ratios, but it increases the PCB routing area. Another well known technique is to introduce a guard trace between the two microstrip lines Fig1(b). However, this technique cannot eliminate FEXT and NEXT completely, the serpentine guard increased the capacitive coupling ratio without altering the inductive coupling ratio and reduced FEXT by about 40% Fig1(c)[1][2]. But still the impact of crosstalk induced jitter was maximum. The parallel stub microstrip lines were proposed to eliminate \(V_{FEXT}\) and \(V_{NEXT}\)[5]. But the NEXT was found increasing at the rate of reducing FEXT, also it required an EMI filter which increased the cost. The proposed sinusoidal structure has been proved to reduce both FEXT and NEXT by 5dB at 6 GHz.
II. ENHANCED STRUCTURE AND EMPIRICAL FORMULATION

The proposed sinusoidal microstrip line consists of unit section of length $T$, repeated in the length direction. This section consists of crest and trough segments. These segments of the aggressor and victim lines are aligned with each other along the direction of length with narrow spacing. The narrow spacing between these segments increases the $C_m$ between the aggressor and victim lines. In this enhanced structure the length of a gap is increased without increasing the length of coupled section Fig2. The main capacitances of the lines remain nearly constant as the surface areas of the lines were not altered.

On the other hand, the increase in fringe capacitances is observed as the counters of the lines have been made longer. The fringe capacitance is the capacitance observed due to the stray electric field at the edges of the lines. It occurs when the electric lines extend the area of the overlap. The self capacitance Eqn(3) of the proposed structure is

$$\frac{C}{l} = \varepsilon_0 \varepsilon_r K_{c1} \frac{W}{H}$$  (3)

The mutual capacitance of the proposed structure is

$$\frac{C_m}{l} = \varepsilon_0 \varepsilon_r K_{c2} \frac{T}{S}$$  (4)

Where $K_{c1}$ and $K_{c2}$ are modeling the fringing the fringing effect on the microstrip lines ($C_{of}, C_{mf}, C_{mfa}$). The main capacitance (3) of the lines is given in terms of line width, correction for fringe capacitance and substrate height. The mutual capacitance Eqn(4) is given in terms of spacing between the lines, metal thickness and the correction for fringing capacitance. After increasing the length of the gap, the new mutual capacitance is

$$\frac{C_m'}{l'} = \varepsilon_0 \varepsilon_r K_{c2} \frac{T}{S}$$  (5)

The Increasing Factor (IF) of the concerned mutual capacitance is

$$IF = \frac{C_m'}{C_m} = \frac{l'}{l}$$  (6)

This is approximated by the line integral Eqn(7) of the coupling profile. In order to make the calculation simpler a sinusoidal profile Eqn(8) was chosen so that the line integral and IF are,

$$l' = \int_T \sqrt{1 + [f'(x)]^2} \, dx$$  (7)

$$IF = \frac{\int_T \sqrt{1 + [f'(x)]^2} \, dx}{T}$$  (8)

The new mutual capacitance Eqn(5) of the proposed structure is observed to be equal to the capacitance possessed by a planar capacitor with length $l'$, height $t$ and gap $s$. The actual capacitance will be greater as the electric field in the gap Fig3 will experience the shortest path and this effect is modeled by a correction factor $K_p$ which is in terms of gap profile function, gap size and its amplitude.

$$IF = K_p \cdot IF$$  (9)

III. RESULTS AND DISCUSSION

In order to assist the objective of mitigating crosstalk, we hereby modify the geometry of the microstrip line. The back papers that had been referred are Parallel microstrip line, Guard trace with ground vias, Double stub microstrip structure, Serpentine structure etc. In our proposed structure, we employ a sinusoidal trace. Some of the above mentioned conventional structures and our proposed structure has been simulated as follows.

While simulating these results, we set the frequency range as 0-6 GHz. For our proposed structure, A/T ratio is varied and then simulated. Among these results the trace with optimum result has been considered and fabricated. Conventional traces such as parallel microstrip line trace and serpentine structure have also been fabricated on the same PCB to make sure that values measured are qualified. For all these traces the dimensions are kept constant and the specification are:

<table>
<thead>
<tr>
<th>W(mm)</th>
<th>L(mm)</th>
<th>S(mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>200</td>
<td>1.5</td>
</tr>
</tbody>
</table>

For the serpentine structure, horizontal and vertical traces have been kept perpendicular to each other as shown in Fig.1©and that forms the trace. As the cross section varies along the trace, it sometimes introduces...
discontinuities. The proposed structure consists of sinusoidal trace with A and T as shown in Fig.2 which are amplitude of the sinusoidal structure and a section of trace, respectively, considered when compared to parallel trace as discussed in the previous chapters. Here, the same sinusoidal format is followed over the entire trace without modification. So that there would no such change of cross section as in case of serpentine and hence no discontinuities along the trace. In this structure, we vary the amplitude value keeping T as constant and hence obtained various A/T ratios. The trace has been varied for each A/T value and this varies from 0 to 0.45, as T=2.5mm and A varies from 0 to 1.125mm. Each trace is varied with respect to the A/T ratio and simulated using ADS software [9].

The simulated outputs consist of $S_{11}$, $S_{12}$, $S_{13}$, $S_{14}$ where these parameters represent the return loss, insertion loss, near-end crosstalk, far-end crosstalk respectively. The results for each structure is shown in Fig.4–Fig.6.
Although various values of A/T show better performance than the conventional structures the results achieved for A/T=0.3 is preferred as the return loss has been reduced by 20dB, insertion loss by 2.2dB, NEXT by 5dB and FEXT by 4 dB Table 2. The comparison of the preferred structure with the conventional is tabulated in Table 2. 

**Table 2. Comparison with conventional performance**

<table>
<thead>
<tr>
<th>Structure</th>
<th>S11</th>
<th>S12</th>
<th>S13</th>
<th>S14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel microstrip</td>
<td>-20</td>
<td>-7</td>
<td>-22</td>
<td>-5</td>
</tr>
<tr>
<td>Serpentine</td>
<td>-15</td>
<td>-7.8</td>
<td>-26</td>
<td>-15</td>
</tr>
<tr>
<td>Sinusoidal</td>
<td>-35</td>
<td>-10</td>
<td>-31</td>
<td>-19</td>
</tr>
</tbody>
</table>

**CONCLUSIONS**

The coupled microstrip lines posses of property of increased near end and far end coupling which resulted in the degradation in performance of the PCB. Hence the proposed sinusoidal modification in the trace geometry has reduced the return loss by 57%, insertion loss by 22%, NEXT by 16% and FEXT by 21% when compared to the existing structures. The reduction depends on the gap profile function parameters. It has been observed that the optimum performance of the modified trace has been achieved when A/t ratio equals 0.3.

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**REFERENCES**


[9] Advanced design system India