A HIGHLY LINEAR LOW NOISE CMOS LNA FOR WIRELESS COMMUNICATION APPLICATIONS

[1]CHINMAY DESHPANDE, [2]SAVITA R. PAWAR

[1]PG Student, MITAOE, Pune.
[2]Asst. Prof, Dept. of Electronics, MITAOE, Pune.
E-mail: [1]chimnay.jd@gmail.com, [2]srpawar@etx.maepune.ac.in

Abstract—In this paper, the design of a highly linear wideband CMOS low-noise amplifier (LNA) for wireless communication applications ranging from 600 MHz to 3 GHz using 0.13-µm technology is described. Here, CMOS inverter based wideband LNA is used in this design. Input Impedance matching is achieved by using negative resistive feedback along with feed-forward topology. The proposed amplifier achieves wideband input matching with S_{11} of less than -10 dB for overall bandwidth range. The designed LNA demonstrates a 33--24dB voltage gain (S21), 1.6—1.9dB noise figure (NF) with IIP3 of +8.02dB. The design drains 13mA of current from 1.2v supply with power consumption of 15.6mW.

Index Terms—CMOS inverter, Low noise, inductorless, Noise Figure, Noise cancelling, Wideband amplifiers.

I. INTRODUCTION

Wireless communication systems (GSM/UTMS/LTE) demands for higher data transfer rates without compromising range of the system. Thus various wireless technology such as Cognitive Radios (CR's), Software Defined Radios (SDR), Wi-Fi, Bluetooth, WiMAX [1]-[4] becomes popular among academic as well as industrial researchers. Most of these technologies operates between 50MHz to 10GHz frequency band. To cover such wide frequency band RF frontend are used as receiver. Also for mobile devices, sharing frontends of various applications can result in reduced power consumption. Thus the behavior of receiver is determined by frontend low noise amplifier. This can be achieved using wideband low noise amplifier. However, it is difficult to achieve such high performance from wideband LNA's as they suffer from various trade-off between some parameters such as noise figure, gain linearity, input matching etc.

Thus considering the necessary requirement we presents low noise amplifier design. The design is based on feed-forward noise cancelling technique using CMOS inverter structure. The design being inductorless has low power consumption and small size makes it more advantageous for modern receiver systems.

II. RELATED WORKS

To overcome the tradeoff between performance parameter various topologies has been developed and used for wideband LNA. For example, the distributed amplifier technique, the filter-type amplifier [3], the common-gate amplifier [4], resistive shunt feedback amplifier [5]. Distributed amplifier provides gain at higher frequency and for that more inductors are used, hence increase in power. Capacitor cross coupling technique [1], noise cancelling technique [2], combination of CG-CS cascade topology [7], [8] are used to obtain low NF. However, all these techniques suffers from disadvantages such as degrading voltage gain, high power consumption, large chip area, nonlinearity, inadequate NF.

In this paper to obtain high gain and low noise figure simultaneously, a CMOS inverter using noise cancelling technique is implemented. We use CMOS inverter for low noise amplifier design. Also, the design is inductorless and capacitorless and thus it improves size and reduces power consumption (very less parasitic capacitance).

III. WIDEBAND LNA CHARACTERISTICS

An LNA combines a low noise figure, reasonable gain, and stability without oscillation over entire useful frequency range. The Low Noise Amplifier (LNA) always operates in Class A, typically at 15-20% of its maximum useful current. Class A is characterized by a bias point more or less at the centre of maximum current and voltage capability of the device used, and by RF current and voltages that are sufficiently small relative to the bias point that the bias point does not shift. The smallest signal that can be received by areceiver defines the receiver sensitivity.

Its main function is to amplify extremely low signals without adding noise, thus preserving the required Signal to-Noise Ratio (SNR) of the system at extremely low power levels. Additionally, for large signal levels, the LNA amplifies the received signal without introducing any distortions, which eliminates channel interference.

A. **Gain**

The forward transducer power gain represents the gain from transistor itself with its input and output presented with 50 ohm impedance. The manufacturer of the transistor at multiple frequencies and different Vce and current levels provides the S21 values. Additional gain can be obtained from source and load

matching circuits. Maximum Stable Gain and Maximum Power Gain (Gmax) are good indicators of additional obtainable gain from the LNA circuit.

B. Noise Figure

Noise figure F is one of the major characteristic for wideband amplifiers. F determines the sensitivity of the system. Lower the value of F higher will be its sensitivity. However, the input impedance matching for wideband LNA is not good enough as compared to narrow band LNA. Low noise figure and good input match is really simultaneously obtained without using feedback arrangements.

$$NF = 10\log_{10}(F) \quad (1)$$

C. Linearity

LNA linearity is another important parameter. A figure of merit for linearity is IP3. A two-tone test is used for derivation of IP3. As a rule of thumb for bipolar junction transistors (BJT), IP3 can be estimated from the following formula:

$$IIP3 = P1dB + 10.5dB \quad (2)$$

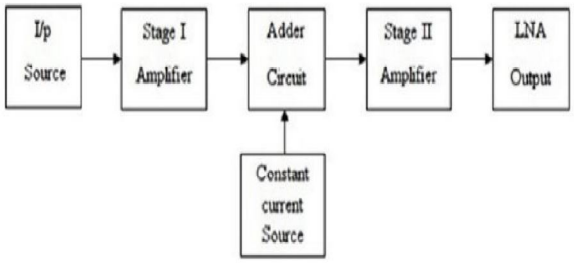

Fig.1. Block Diagram of proposed Design.

Based on the theory explained in section II, block diagram of proposed design is shown in fig. It consists of following functional blocks. 1) Stage I amplifier provides necessary input impedance matching, $Z_{IN} = R_S$; 2) Adder circuit along with constant current source functions as noise cancelling circuit. Constant current is an auxillary amplifier required as reference signal. 3) Stage II amplifier provides necessary gain and linearity to the system.

IV. WIDEBAND LNA IMPLEMENTATION

A Wideband CMOS low noise amplifier is implemented in TSMC 0.13µm technology using Agilent's ADS 2009 software. The schematic of proposed design is shown in fig. Transistor M1, M2 forms CMOS inverter. R1 is feedback resistor. M1, M2 transistor forms a CMOS inverter with a negative feedback resistor. Using this method M2 transistor will adapt the voltage level of M1 transistor and is called as self-biasing. Transistor M2 is main source of intrinsic noise in the circuit. Transistor M5 and M6 is adder circuit. Also, a constant current source is used as an auxillary amplifier to realize gain of feed-forward path $G \approx 1$without extra noise, power consumption and distortion. Adder circuit will add phase shifted noise signal with reference signal and thus will suppress noise from the original signal. The noiseless output is then amplified in stage II to achieve high gain and improved linearity.

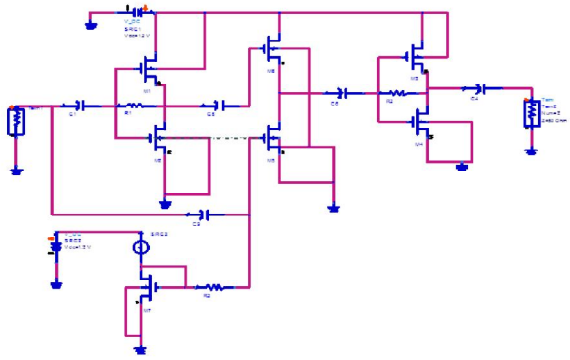

Fig.2. Schematic of implemented design

V. SIMULATION RESULTS

In order to design LNA various optimization techniques are consider to satisfy all its design requirements. Therefore, the LNA was initially simulated for its biasing characteristics to obtain its suitable operating point. The simulation is carried out for a broadband response. The broadband response runs from 0.6 to 6 GHz while the operating bandwidth is from 0.6 to 3 GHz.This is done to check the behaviour of design with increasing bandwidth. Based on the proposed design of LNA simulation testing is done using Agilent's ADS and its layout has been developed. Simulation results, for explanation are obtained on 2.4 GHz and it is carried out in two stages; 1) small signal analysis: to obtain gain, NF, insertion loss, input return loss and stability. 2) Harmonic balance testing: to obtain 1dB compression point (P1dB). The design is tested for both with and without noise cancellation. This is done by removing feedback capacitor C8. It has been observed that NF and voltage gain has been improved by 0.4-0.6dB and 5-7dB respectively. The simulation results are explained as follows:

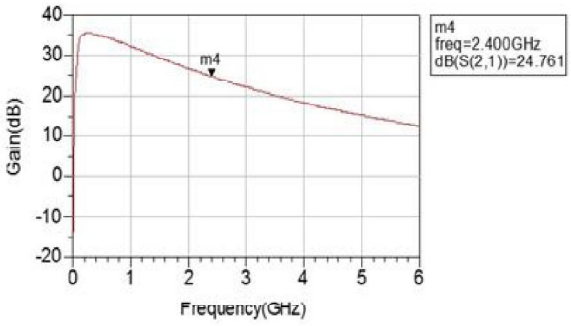

Fig.3. Gain response of the design.

Fig. 3. Shows gain achieved by the proposed design. Gain of this system varies from 35dB at 600MHz to 22dB at 3GHz and 24.7dB at 2.4GHz. For low noise

amplifier gain should be as high but it degrades at higher frequencies. Therefore to achieve higher gain amplifiers are used in stages.

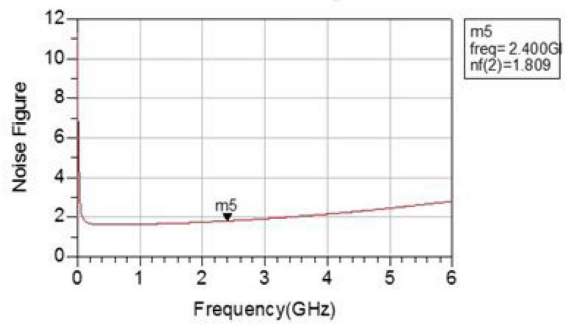

Fig. 4. Noise figure achieved for the design

Fig. 4 shows NF, ranges from 1.5dB to 2dB for the overall operating bandwidth while at 2.4GHz NF is 1.8dB. Ideally, noise figure should be less than 3dB. The noise figure achieved is much less than 3dB. Also it can be seen that as the frequency increases NF also gets increased. Still with increasing frequency the NF of this remain below 3dB up to 6GHz. Fig.5 shows reverse isolation characteristic of LNA. An ideal LNA has infinitereverse isolation. However, reflected signals can pass through the amplifier in the reversedirection. Therefore, reverse isolation is important to quantify. The reverse isolationachieved is -64dB.

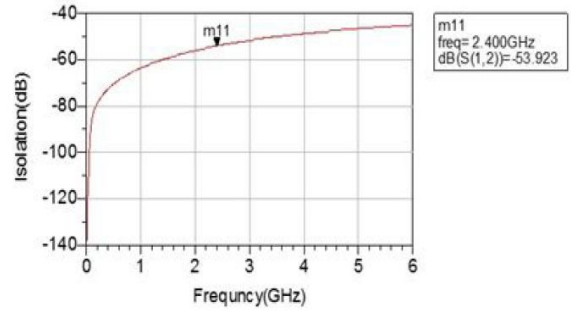

Fig. 5. Isolation loss

Fig 6 shows the input and output return loss. The S11 and S22 parameter is plotted over the frequency. It improves the impedance matching of input and output. When some amount of power is given to the input it should drives to output but practically some amount of input power comes out of input. This is called as input return loss.

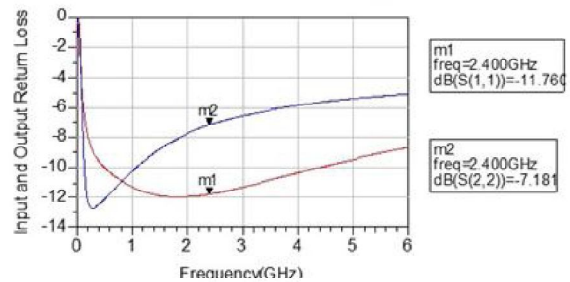

Fig. 6. Input and Output return loss

Fig. 7 and 8 P1dB compression results. An amplifier is called linear when the output power increases linearly with the input power. The ratio of these two powers is the power gain G. as input power increases, the amplifier transfer function becomes nonlinear, that is the output power is lower than predicted by the small signal gain. This nonlinear behaviour in amplifiers introduces distortion in the amplified signal. The output power at which the gain has dropped by 1 dB below the linear gain is called the 1 dB compression point, P1dB. The P1db is -1.78.

Fig. 7 shows the input power level when gain is drop by 1dB. To obtain 1dB compression point output power is plotted versus input power. Input power at which gain drops by 1dB is marked and P1dB is obtained which is -1.78dB. IIP3 is calculated using the thumb rule equation (2). Therefore P1db +10.5= 8.72 at high gain.

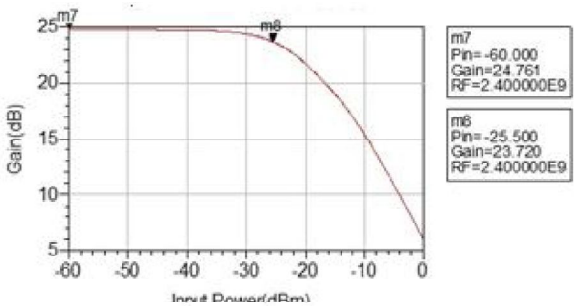

Fig. 7. 1db compression

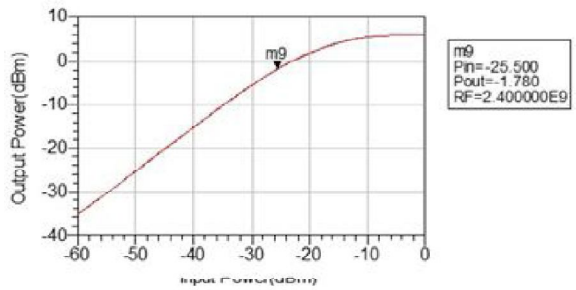

Fig. 8. P1dB compression point.

Table 1: Performance Comparison of the implemented and previously reported VGAs

Ref.	Tech (µm)	S21 (dB)	NF (dB)	S11 (dB)	IIP3 (dB)	PD (mW)	year
[1]	0.13	11.2	2.5	-10	-2.7	1.9	2007
[2]	0.35 Si-Ge	12.3	2.1	-	2.5	13.2	2008
[3]	0.18	19.3	3.5-4.7	-11	-14	30.6	2009
[5]	0.18	18.4	2.1-3.2	-16	-	17.4	2011
[8]	0.18	35	1.2	-11	-11	16.4	2009
This Work	0.13	33 -24	1.6– 1.9	-10	8.02	15.6	2015

CONCLUSION

A Highly Linear Low Noise CMOS LNA for Wireless Communication Applications is presented in this paper. Experimental results show that this technique

improves the Linearity, NF, gain, and power dissipation of LNA, especially for LNA design in scaling down CMOS technology. The results achieved are simulated results, obtained on Agilent's ADS 2009 and its core layout was designed using Micro-Wind software.

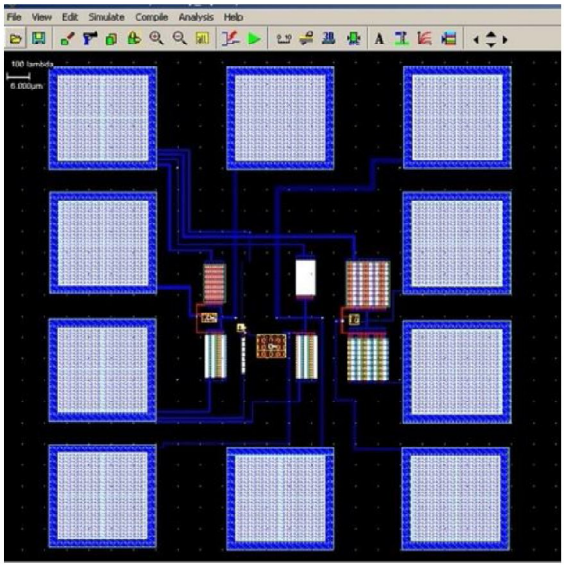

Fig. 9. Layout of design

Fig. 9 shows layout of design. The size of layout is 100.5µm X 118µm.

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