

# DESIGN AND FPGA IMPLEMENTATION OF SLIDING MODE CONTROLLER FOR BUCK CONVERTER

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**Abstract**—This paper presents the digital design of Sliding Mode Controller (SMC) for synchronous buck converter for high switching frequency and low power application. The buck converter is designed for a voltage mode control with PWM technique having switching frequency of 3MHz. It will step down the input voltage of 3.6V to output voltage of 0.9V with duty ratio of 25% and maximum load current of 800mA. The buck converter output voltage is maintained constant irrespective of load variations. The digital SMC is implemented on Spartan 3E FPGA Kit using Xilinx System Generator Tool. Using digitally controlled SMC, an Undershoot of 0.33% for load variations of 0.4A to 0.6A and 1.11% for load variations of 0.4A to 0.8A with very fast Settling Time of 2.5 $\mu$ s is achieved.

**Index Terms**— Synchronous buck converter, Digital SMC, Spartan 3E FPGA Kit, Xilinx System Generator Tool, Undershoot and Settling Time.

## I. INTRODUCTION

When compared to linear power supplies, switching mode power supplies (SMPS) provide easy integration, high efficiency, small dimensions and weight. SMPS have been widely used in numerous portable communication systems such as smart phones, digital cameras, tablets, navigation systems, medical equipment and other low power devices. Typically these devices require several independent supply voltages each usually different from the voltage supplied from the battery or external ac to dc power supply. In all these portable devices a constant supply voltage is required for proper operation of the chips. Hence there is a need to maintain a constant supply voltage irrespective of changes in load current. Due to many disadvantages of using analog control in DC-DC SMPS, the present trend is to go for digital control in DC-DC SMPS. Some of the advantages of digital control include Advanced control algorithm implementation, Flexibility and programmability, Size miniaturization and high frequency, Less susceptible to component and variations, which is a not possible using analog control techniques.

In this paper a digital sliding mode (SM) controlled buck converter for low power applications is presented. The buck converter is modeled using Matlab-Simulink. The SMC is also incorporated into the buck converter for closed loop operation. A comparison of open loop buck converter and SMC controlled buck converter is made with respect to their transient response using Matlab-Simulink.

This paper is organized as follows. Section II reviews Voltage mode control of DC-DC converter. Section III discusses Digital control in DC-DC SMPS. Section IV explains Synchronous buck converter design. Section V explains the digital design of SMC. Section VI shows Simulation results of open loop buck converter and SMC controlled buck converter. Section VII shows the FPGA implementation of SMC

and hardware-software co-simulation. Section VIII summarizes main results of this paper.

## II. VOLTAGE MODE CONTROL OF DC-DC CONVERTER

Fig.1 shows the Voltage mode control of DC-DC converter using SMC as compensator [1].  $V_{in}$  is the input voltage,  $V_o$  is the output voltage.  $V_o$  is compared with the reference value of voltage  $V_{ref}$ . If  $V_o$  is equal to  $V_{ref}$  then the error is zero. If  $V_o > V_{ref}$  or  $V_o < V_{ref}$  then corresponding error signal  $V_e$  will be generated as  $V_e = V_{ref} - V_o$ . The error signal  $V_e$  is fed to the compensator block which in turn generates a signal  $V_c$  that is proportional to the duty ratio  $d$ . This  $V_c$  is compared with a constant switching saw tooth waveform using a comparator. The pulse will be generated and this pulse which is directly proportional to  $d$  will be given to the DC-DC converter, which drives the switches of the DC-DC converter and there by maintains the inductor voltage constant and thus the output voltage remains constant which will be now equal to the reference value.

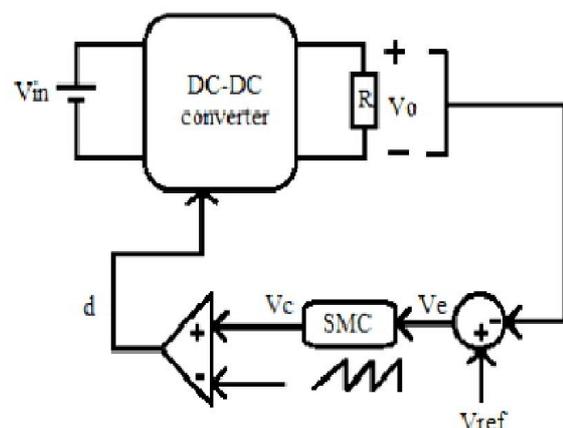


Fig.1. Voltage Mode Control of DC-DC Converter

### III. DIGITAL CONTROL IN DC-DC SMPS

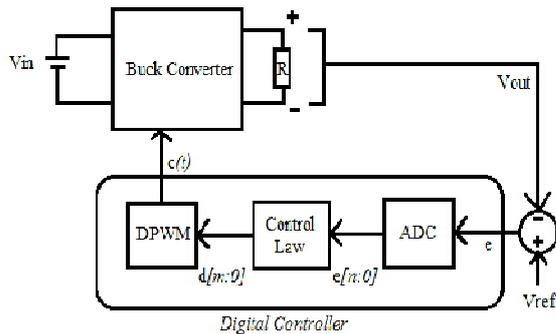


Fig.2. Block Diagram of Digitally Controlled Buck Converter

Fig.2. shows the block diagram of digitally controlled buck converter [2]. The digital controller consists of three blocks ADC, Control Law and Digital PWM (DPWM) as shown in the figure. The output voltage  $V_{out}$  is compared with the reference value  $V_{ref}$  and the error signal which in analog in nature will be generated if  $V_{out} < V_{ref}$  or  $V_{out} > V_{ref}$ . If  $V_{out}$  is equal to  $V_{ref}$  then error  $e$  will be zero. As SMC is a digital controller the analog error signal  $e$  should be converted into digital/discrete signal. This is done with the help of Analog to Digital converter (ADC). The control Law block generates a discrete signal which is proportional to the duty ratio. This discrete signal  $d[m:0]$  is given to DPWM block where in the discrete signal is converted back into analog signal  $c(t)$  to drive the switches of the buck converter, thus the output voltage is maintained constant such that  $V_{out}$  conforms to the reference value  $V_{ref}$ .

### IV. SYNCHRONOUS BUCK CONVERTER DESIGN

This section covers buck converter topology with a fixed switching frequency, pulse width modulation (PWM) and operation in the continuous current mode (CCM) [3]. Four design parameters are required. 1. Input voltage  $V_{in}$  of 3.6V, 2. Output voltage  $V_{out}$  of 0.9V, 3. Maximum output current  $I_{out(max)}$  of 800mA and 4. Converter's switching frequency  $f_{sw}$  of 3MHz. Fig.3 illustrates the circuit and basic components for a buck converter

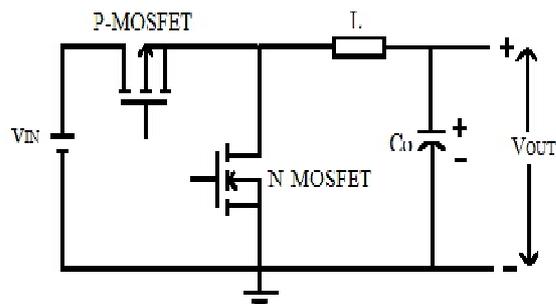


Fig.3. Buck Converter Circuit.

#### A. Inductor Selection:

The buck converter is assumed to be operating in CCM and it implies that inductor does not fully discharge during the switch-off time. Eq(1) gives minimum value of inductor.

$$L = (V_{in} - V_{out}) \times \frac{V_{out}}{V_{in}} \times \frac{1}{f_{sw}} \times \frac{1}{LIR \times I_{out(max)}} \quad (1)$$

Where  $f_{sw}$  is the buck converter switching frequency and LIR is the inductor current ratio expressed as a percentage of  $I_{out}$ . An LIR of 0.2 represents a good tradeoff between efficiency and load transient response.

Peak current through the inductor determines the inductor's required saturation-current rating, which in turn dictates the approximate size of the inductor. Inductor's peak operating current is calculated as follows:

$$I_{peak} = I_{out(max)} + \frac{\Delta I_{inductor}}{2} \quad (2)$$

Where,

$$\Delta I_{inductor} = LIR \times I_{out(max)} = (V_{in} - V_{out}) \times \frac{V_{out}}{V_{in}} \times \frac{1}{f_{sw}} \times \frac{1}{L}$$

#### B. Output Capacitor Selection:

Output capacitance is required to minimize the voltage overshoot and ripple present at the output of a buck converter. Large overshoots are caused by insufficient output capacitance, and large voltage ripple is caused by insufficient capacitance as well as a high equivalent series resistance (ESR) in the output capacitor. The ESR values must be as low as possible to reduce the ripple in the output voltage. The output capacitance  $C_o$  is calculated as follows.

$$C_o = \frac{L \left( I_{out(max)} + \frac{\Delta I_{inductor}}{2} \right)^2}{(\Delta V + V_{out})^2 - (V_{out})^2} \quad (3)$$

ESR of the output capacitor dominates the output voltage ripple. The amount can be calculated as follows:

$$V_{out(ESR)} = I_{(ripple)} \times ESR(C_o) = \Delta I_{inductor} \times ESR(C_o) \quad (4)$$

### V. DESIGN OF SLIDING MODE CONTROLLER

Sliding mode control (SMC) was introduced initially for the robust control of variable structured systems (VSS). VSS are systems physically changed intentionally during time with respect to the structure control law. SMPS converters are non-linear system in nature due to their switching property and SMC is also a non-linear controller.

The basic principle of SMC is to employ a certain sliding surface as a reference path, such that the state variables trajectory can be directed towards the desired equilibrium. The purpose of the switching control law is to drive the nonlinear plant state trajectory onto a pre-specified (user-chosen) surface in the state space and to maintain the plant state trajectory on this surface for subsequent time [4]. The

main idea of SMC is to bring and keep the error on a sliding surface such that the system is insensitive to the disturbances and parameter changes.

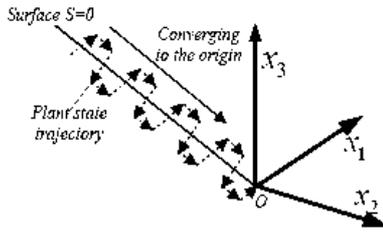


Fig. 4. Graphical representation of SMC process

The SMC design approach consists of two components: The first step is to build a sliding surface with different control objectives and the second step is to determine the existence of sliding motion and ensure the stability. Fig.4 shows the graphical representation of the plant state trajectory behavior in SMC process.

A. System modeling for PWM based SMC:

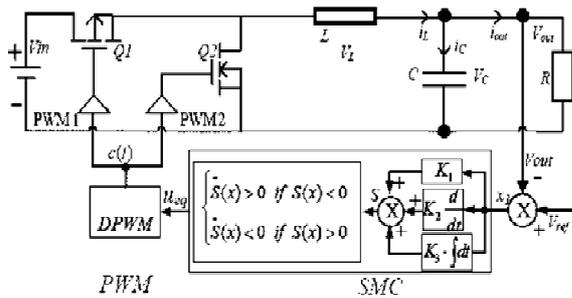


Fig.5. The schematic diagram of a PID-type SMC for a digitally controlled buck converter

The first step to the design of a SMC is to determine the state variables in terms of the desired SMC [5]. The sliding mode controller involves the output voltage error and its integral and differential portions. Besides the differential portion, it also takes into account an additional voltage error integral term to reduce the steady-state dc error of the output voltage. If the output voltage of buck converter  $V_{out}$  less than the reference value  $V_{ref}$ , the error  $x_1$  is positive. The error signal  $S$  is proportional to the error signal  $x_1$  which means  $S(x) > 0$ . The error is above the sliding surface as shown in Fig.4. The error has to be brought back to the sliding surface such that the rate of change of error signal  $S(x)$  should be less than zero. So SMC will generate a discrete signal  $U_{eq}$  which is proportional to the duty ratio of the converter and thus the error is minimised by increasing the on time of the switch  $Q1$  and thus the output voltage remains constant.

If the error is negative that means the error is below the sliding surface as shown in Fig.4 then the error has to be brought back to the sliding surface such that the rate of change of  $S(x)$  should be greater than zero. Hence, SMC will generate a signal  $U_{eq}$  which is

proportional to the duty ratio of the converter and thus the error is minimised by decreasing the on time of the switch  $Q1$  and thus the output voltage remains constant [6,7].

In Fig.5 the output voltage  $V_{out}$  is the SMC control objective,  $K = [K_1, K_2, K_3]^T$  is the sliding parameter of SMC and the control variable  $x$  can be expressed as:

$$x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} V_{ref} - V_{out} \\ \frac{d}{dt}(V_{ref} - V_{out}) \\ \int (V_{ref} - V_{out}) \end{bmatrix} \quad (5)$$

The equivalent control signal  $u_{eq}$  is thus obtained by setting  $\dot{S}(x) = 0$ ,

$$U_{eq} = \frac{1}{V_{in}} \left[ V_{ref} - LC \left( \frac{K_1}{K_2} - \frac{1}{RC} \right) \frac{dV_{out}}{dt} + LC \left( \frac{K_3}{K_2} - \frac{1}{LC} \right) (V_{ref} - V_{out}) \right] \quad (6)$$

Where  $U_{eq}$  is continuous and equals to PWM duty ratio  $d$  and parameters  $K_1/K_2$  and  $K_3/K_2$  are to be determined which corresponds to the desired SMC dynamics.

$$\frac{K_1}{K_2} = \frac{4\pi f_{sw}}{15} \quad \text{and} \quad \frac{K_3}{K_2} = \frac{4\pi^2 f_{sw}^2}{15^2} \quad (7)$$

VI. SIMULATION RESULTS

The simulation of open loop buck converter and SMC controlled buck converter is performed using Matlab-Simulink software. The results of both open loop and closed loop are compared.

Fig.6 shows the Matlab-Simulink model for open loop buck converter. The buck converter block and PWM block is modeled using subsystem in Simulink. The input voltage of 3.6V is given to the buck converter with duty cycle of 25% and the load current is varied from 0.4A to 0.8A.

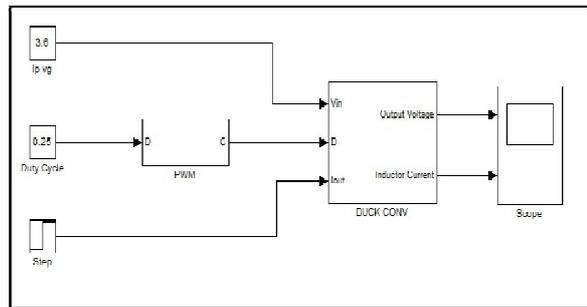


Fig.6. Simulink model for open loop buck converter

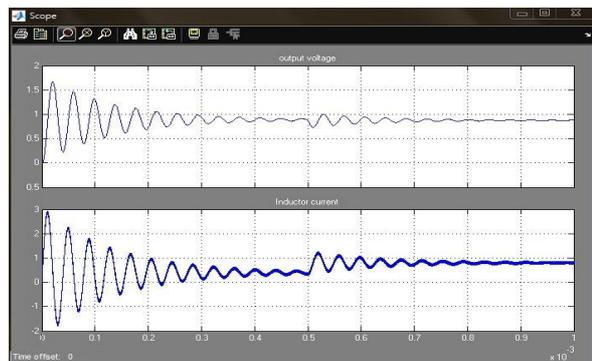
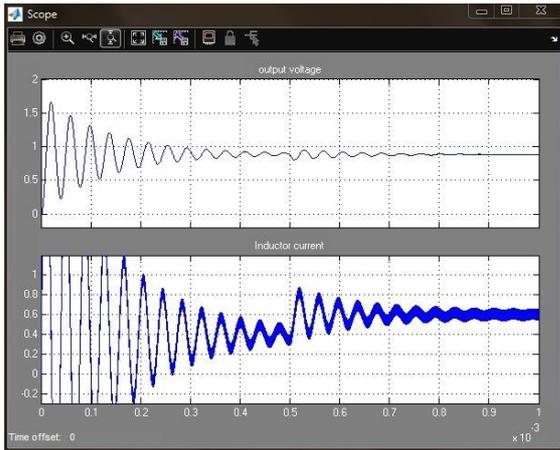


Fig.7. Simulation results for open loop buck converter for load variations from 0.4A to 0.8A

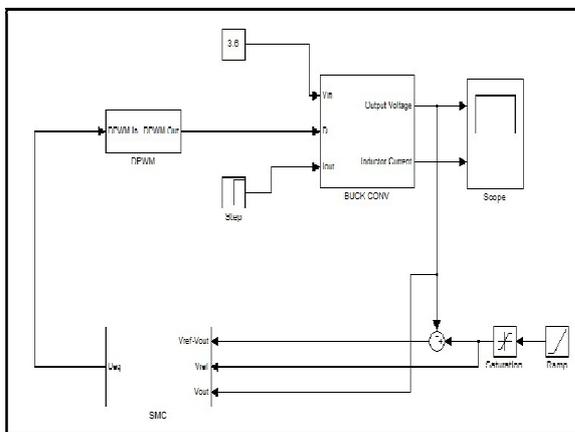


**Fig.8. Simulation results for open loop buck converter for load variations from 0.4A to 0.6A**

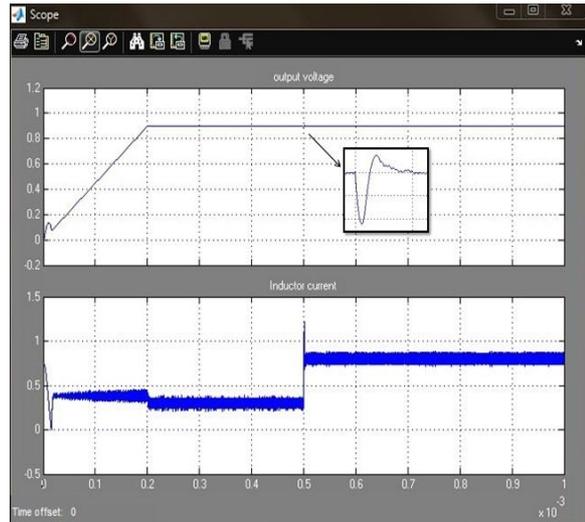
Fig.7 shows the simulation results of open loop buck converter. We can observe that the output voltage is having an undershoot of 17.77% with settling time of 350µs for load variations from 0.4A to 0.8A. Fig.8 shows the simulation results for load variations from 0.4A to 0.6A having undershoot of 11.11% with settling time of 400µs.

Fig.9 shows the Matlab-Simulink model for SMC controlled buck converter. The buck converter block, SMC block and DPWM block is modeled using subsystem in Simulink. The output voltage from the buck converter is compared with the reference value  $V_{ref}$  of 0.9V and the error is converted into discrete signal which is then given to the sliding mode controller. The DPWM block converts the discrete PWM value from SMC block into analog PWM signal that is continuous in nature which drives the switches of buck converter and thus maintains the output voltage to be constant irrespective of load current variations.

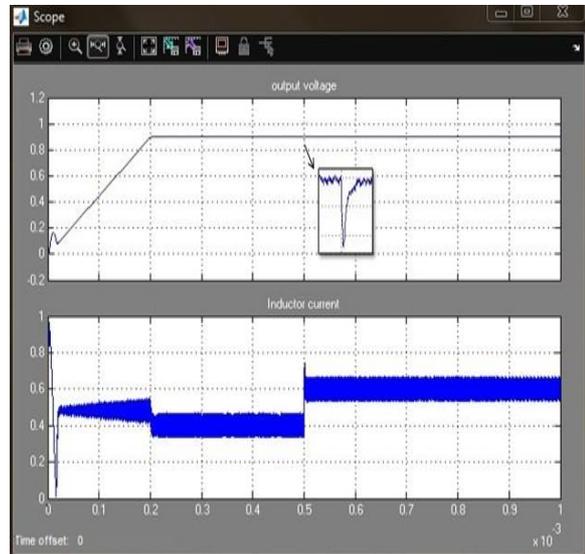
Fig.10 shows the simulation results of SMC controlled buck converter. We can observe that the output voltage is having an undershoot of 1.11% with settling time of 2.5µs for load variations of 0.4A to 0.8A. Fig.11 shows the simulation results for load variations from 0.4A to 0.6A having undershoot of 0.33% and settling time of 2.5µs .



**Fig. 9. Simulink model for SMC controlled buck converter**



**Fig.10. Simulation results for closed loop buck converter for load variations from 0.4A to 0.8A**



**Fig.11. Simulation results for closed loop buck converter for load variations from 0.4A to 0.6A**

## VII. FPGA IMPLEMENTATION AND HARDWARE CO-SIMULATION

The hardware-software co-simulation of SM controlled buck converter is performed in Matlab/Simulink environment using Xilinx system generator tool. It is performed to validate the design operating on FPGA. The digital SM controller, Spartan 3E board with the XC3S500E-4FG320 FPGA. Fig. 12 shows the modeling of digitally controlled buck converter in simulink. Fig. 13 shows the system generator based Sliding mode controller for buck converter.

Before performing hardware-software co-simulation, a simulink library is to be created containing new hardware co-simulation block. The hardware implementation is then executed by connecting the board to the PC, thereby, closing the loop. The Xilinx ISE program then generates the bit file and loads it into FPGA through a standard JTAG connection. Fig.

14 shows the hardware-software co-simulation model of digital controller.

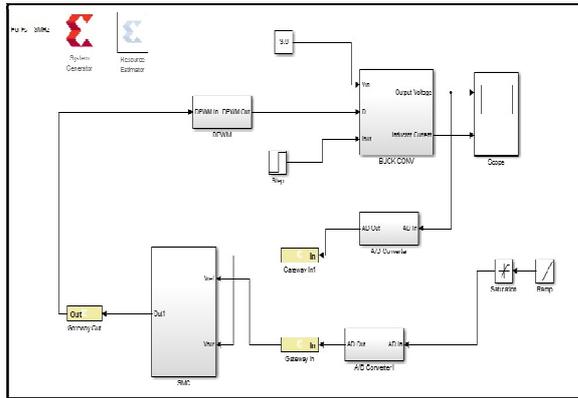


Fig.12 The modeling of digitally controlled buck converter

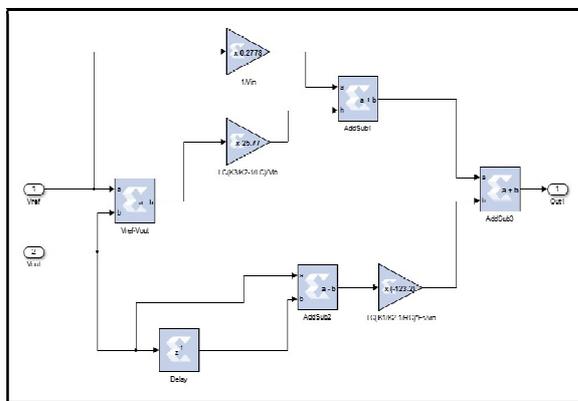


Fig.13 Sliding mode controller implementation through xilinx system generator.

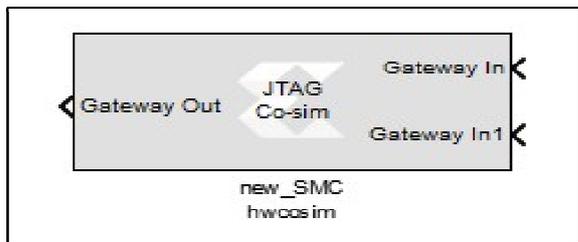


Fig. 14 Hadrware/software co-simulation block for the controller

One of the most important analysis performed during FPGA implementation is timing analysis. The System Generator timing analysis tool can be used to perform timing analysis. It clearly displays the specific paths that will fail in hardware. The slack parameter should not be negative. Fig. 15 shows the timing analysis report for the design.

The time-domain behavior of digitally controlled buck converter is studied in MATLAB/Simulink environment. Fig. 16 shows the co-simulation results for load variations 0.4A to 0.8A and Fig. 17 shows the co-simulation results for load variations from 0.4A to 0.6A and it matches with that of the output which was earlier simulated using all Simulink blocks.

Constraint	Check	Worst Case	Best Case	Timing	Timing
		Slack	Achievable	Errors	Score
TU_hwcoosim_sys_clk = PERIOD TIMEGRP "hwco" SETUP		0.044ns	18.956ns	0	0
sin_sys_clk 50 MHz HIGH 50%	HOLD	0.999ns		0	0
TS_d TO U = MAXDELAY FROM TIMEGRP "U_CLK" SETUP		10.426ns	4.574ns	0	0
TU_TIMEGRP "U_CLK" 15 ns					
TS_clk_6a3da264 = PERIOD TIMEGRP "clk_6a3" MINPERIOD		18.348ns	1.652ns	0	0
dat64 20 ns HIGH 50%					
NET "jtag_iface/drebl" PERIOD = 30 ns HIGH SETUP		28.167ns	6.833ns	0	0
T 50%	HOLD	1.016ns		0	0

Fig 15. Timing Report

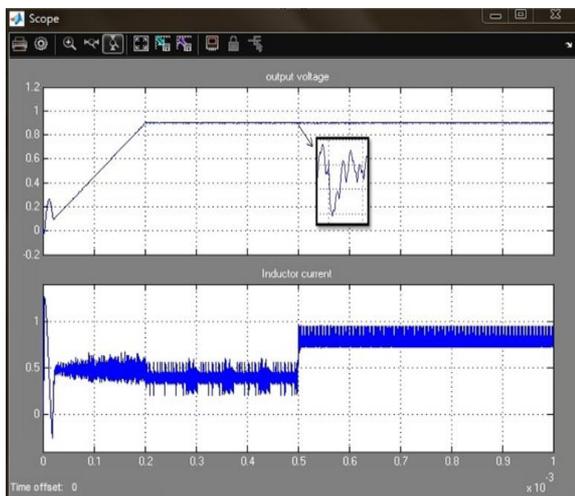


Fig. 16 Co-simulation results for load variations from 0.4A to 0.8A

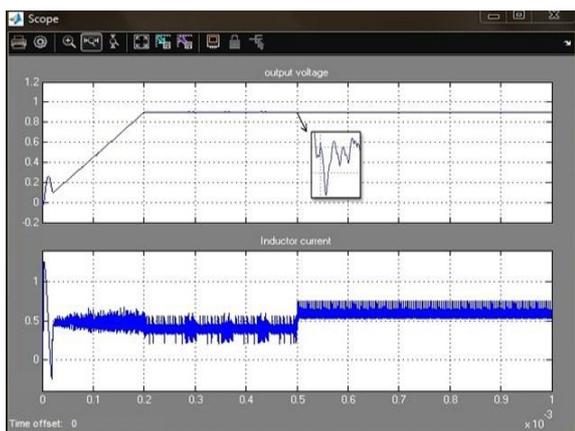


Fig. 17 Co-simulation results for load variations from 0.4A to 0.6A

Table 1 gives the comparison of dynamic response of open loop buck converter and SM controlled buck converter for various load conditions. It is observed that Sliding mode controller provides consistent performance when compared to open loop buck converter. This validates the robustness and good dynamic characteristics of SM controller.

**TABLE 1: COMPARISON OF DYNAMIC RESPONSE OF OPEN LOOP BUCK CONVERTER AND SM CONTROLLED BUCK CONVERTER**

Load variation	Parameters	Open loop buck converter	SM controlled buck converter
0.4A to 0.8A	Maximum peak undershoot	17.77%	1.11%
	Settling time( $\mu$ s)	350	2.5
0.4A to 0.6A	Maximum peak undershoot	11.11%	0.33%
	Settling time( $\mu$ s)	400	2.5

## CONCLUSIONS

In this paper, the digital design of SMC for buck converter for switching frequency of 3MHz with output voltage of 0.9V is performed. The load current is varied from 0.4A to 0.6A/0.8A. Both open loop and closed loop system models are simulated using Matlab-Simulink and compared. The hardware implementation of SMC using Xilinx System Generator with Spartan 3E XC3S500E-4FG320 FPGA has been successfully performed and the results are verified with Simulink environment. It is observed that SM controlled buck converter gives good dynamic response when compared to open loop buck converter. The undershoot has been reduced from 11.11% to 0.33% with load variations from 0.4A to 0.6A and from 17.77% to 1.11% with load variations from 0.4A to 0.8A. Also, the SMC has a

very fast setting time of 2.5 $\mu$ s when compared to open loop buck converter.

Hence SMC is preferred to control the output voltage of buck converter due to the following advantages: It is robust as it is insensitive to load disturbances and uncertainties, easy to design and implement, shows good stability for large load variations and SMC has fast dynamic response.

## REFERENCES

- [1] Sujata Verma, S.K Singh and A.G. Rao, "Overview of control Techniques for DC-DC converters", Research Journal of Engineering Sciences, ISSN 2278 – 9472, Vol. 2(8), 18-21, August (2013)
- [2] Shuibao Guo, Yanxia Gao, Yanping Xui, Xuefang Lin-Shi, and Bruno A, "Digital PWM Controller for High-Frequency Low-Power DC-DC Switching Mode Power Supply," in IEEE 6th International Power Electronics and Motion Control Conference (IPEMC 2009), pp 1340-1346.
- [3] Buck-Converter Design Demystified by Donald Schelle and Jorge Castorena, Technial Staff, Maxim Integrated Products, Sunnyvale, Calif.
- [4] Siew-ChongTan, Y.M.Lai, MartinK.H.Cheung, and ChiK.Tse, "A pulse-width modulation based Sliding mode controller for Buck converter," 35<sup>th</sup> Annual IEEE power electronics Specialist conference , pp.3647-3653,2004.
- [5] Shuibao GUO,Xuefang LIN-SHI,Bruno ALLARD,Bo LI,Yanxia GAO and Yi RUAN,"A FPGA- prototype of a sliding-mode-controller IC for High-Switching-Frequency DC-DC Converters," pp.2895-2900, IECON 2009.
- [6] S.Tan,Y.Lai,andC.Tse,"General design issues of sliding-mode controllers in DC-DCconverters, " IEEETransactions on Industrial Electronics,vol.55, no.3, pp.1160–1174, 2008.
- [7] Alexander G. Perry, Guang Feng , Yan-Fei Liu, P.C. Sen,"A new sliding mode like controlmethod for buck converter," 35<sup>th</sup> Annual IEEE power electronics Specialist conference , pp.3688-3693,2004.

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