COMPARATIVE STUDY OF PWM TECHNIQUES FOR DIODE-CLAMPED MULTILEVEL-INVERTER

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Abstract—Multi-level inverter has emerged as an attractive choice in the field of medium and high power applications. Multilevel inverter synthesizes the staircase voltage waveform from several DC sources which has reduced harmonic content. Multi-level inverter reduces dv/dt, switching losses. A comparative study of various PWM schemes for diode-clamped five-level inverter with three phase induction motor as a load is presented in this paper. A Matlab Simulink model is created and simulated using various PWM control schemes. These schemes are compared for THD analysis.

Keywords—DCMLI, SPWM, SVPWM, PD, POD, APOD, THD.

I. INTRODUCTION

An inverter converts DC input voltage into AC output voltage of variable magnitude and frequency. Recently induction motor is widely used in buildings and industries because of its compact size, endurance and cheap price. However, industrial requires improving its efficiency and to save energy. The inverter with voltage levels three or more are referred as multi-level inverter. Multi-level inverter is effective for large capacity AC motor drives. Harmonic content decreases as the number of level increases thus reducing the filtering requirements. To improve the harmonic characteristics, a five-level inverter could be modulated by a multilevel carrier technique such as four-level carrier modulation. Multi-level pulse width modulation (PWM) inverters are gaining importance due to the fact that lower order harmonics in the output waveforms can be eliminated without any increase in the high order harmonics.

This paper presents a comparative study of five level diode clamped inverter with constant switching frequency for sinusoidal PWM (SPWM) and carrier space vector PWM (SVPWM) with phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition method (APOD). Space vector pulse Width Modulation (SVPWM) has been studied extensively during the past decades. Many different PWM methods have been developed to achieve the following aims: wide linear modulation range, less switching loss, less total harmonic distortion (THD) in the spectrum of switching waveform and easy implementation and less computation time. For a long period, carrier based PWM methods were widely used in most applications [3]. For achieving good response and control of switching, various control schemes are used such as PD, POD and APOD. The performance of each Technique has been investigated based upon reduction in THD [6]-[7].

Progress in the power electronics technology leads to a significant increase in nonlinear loads connected to AC distribution systems. Nonlinear loads are sources of harmonic currents and cause a number of unwelcome effects, like harmonic distortion of line voltages, over voltages, equipment overheating, malfunction, and damage.

The two main techniques of PWM generation for multilevel inverters are sine-triangle PWM (SPWM) and space vector PWM (SVPWM). Multilevel SPWM involves the comparison of a reference signal with a number of level shifted carriers to generate the PWM signal.

II. PRINCIPLE OF OPERATION OF DCMLI

The neutral clamped inverter, also known as diode clamped inverter. The basic architecture of this inverter is as shown in below Fig. 1. The diode-clamped multi-level inverter (DCMLI) is the most extensively applied multilevel converter topology at present. It can reduce harmonics in both of the output voltage and current. Depending on the topology, the multilevel inverters are mainly classified as diode clamped, flying capacitor, and cascaded H-bridge with separate DC source multilevel inverter. The clamping diode eliminates equalization circuits [8]. Diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the more number of capacitors. But the cascaded inverters have the simplest structure [1]. The diode clamped inverter has drawn much interest in motor drive applications because it needs only one common voltage source. Also simple and efficient PWM algorithms have been developed for it [2]. The five level diode clamped inverter delivers the staircase output voltage using five levels of DC voltages developed by DC capacitors [13]. If N is the number of level, then the number of capacitors required on the DC bus are (N-1), the number of power electronic switches per phase are 2(N-1) and the
number of diodes per phase are (N-2)(N-1) [1]. The DC bus voltage is split up for five levels using four capacitors C1, C2, C3 and C4. The voltage across each capacitor is \( V_{dc}/4 \) and each generated phase voltage, e.g. \( V_a \) has five levels with respect to DC side point ‘o’, i.e\( V_{dc}, 3V_{dc}/4, V_{dc}/2, V_{dc}/4 \) and 0 [9]. The voltage stress across each switch is limited to one capacitor voltage through clamping diodes. For multi-level inverter as the number of levels increase the harmonic distortion decreases and efficiency of the inverter increases because of the reduced switching losses.

A n-level three phase DCMLI typically consists of capacitors or DC voltage sources and has \( N^3 \) switching combinations. For five-level DCMLI with DC bus voltage, the voltage across each capacitor is \( V_{dc}/4 \). Thus the voltage stress on each switch will be, \( V_{dc}/4 \) through clamping diode. Table:1 gives output pole voltage and their corresponding switching state.

### Table 1: DCMLI Switching Scheme

<table>
<thead>
<tr>
<th>( V_{an} )</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S1'</th>
<th>S2'</th>
<th>S3'</th>
<th>S4'</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{dc}/2 )</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( V_{dc}/4 )</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<td>1</td>
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<tr>
<td>( V_{dc}/4 )</td>
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<tr>
<td>( V_{dc}/2 )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

### III. CONTROL TECHNIQUES OF MLI

There are various schemes used for controlling multi-level inverter such as

a. Sinusoidal Pulse Width Modulation (SPWM)
b. Third harmonic injection Pulse Width Modulation (THI-PWM)
c. Space Vector Pulse Width Modulation (SVPWM)
d. Selective Harmonic Elimination (SHE-PWM)

### A. Sinusoidal Pulse Width Modulation (SPWM):

Pulse width modulation is used for inverter output voltage control and if we switch a device in a particular fashion harmonics can be eliminated. Using SPWM technique we could push the predominant harmonics to a high frequency till the rated frequency but the utilization of DC link voltage source reduces. In SPWM we compare the carrier signal of high frequency with modulating signal of desired frequency. By increasing the switching frequency we can reduce the lower order harmonics from the output voltage. The SPWM technique is further classified as PD, POD, APOD. These methods generate similar ac-side phase –and line voltage wave-forms. However, the PD technique generates a relatively lower total harmonic distortion. The analysis and the development model are equally valid for PD, POD and APOD techniques [10]. For diode clamped five level inverter four triangular carrier signals are needed. The carriers have the same frequency \( f_c \) and the same peak to peak amplitude. At every instant each carrier is compared with the modulating signal. Each comparison switches the switch ‘ON’ if the modulating signal is greater than the triangular carrier wave assigned to that switch. Fig. 2, 3 and 4 shows the carrier signals for power devices S1, S2, S3 and S4 of the five-level inverter shown in Fig. 1. Gating signals are generated by comparing the sinusoidal waveform. The SPWM phase output voltage results from the comparison of the modulating wave with the four high frequency triangular carrier waves. the three sine modulating waves for three phases, are phase shifted to each other by 120° and are expressed by –

\[
V_m, x = m \sin(\alpha t + j \frac{2\pi}{3}) \tag{1}
\]

\[
m = \frac{A_m}{A_{u1} + A_{u2} + A_{l1} + A_{l2}} \tag{2}
\]

\[
m_f = \frac{f_c}{f_m} \tag{3}
\]

Where,

\( j = 0, -1, +1 \)

\( x = a, b, c \)

\( m \) = modulation index

\( m_f \) = frequency ratio

\( f_c \) = carrier wave frequency

\( f_m \) = modulating wave frequency

\( A_m \) = modulating wave peak-to-peak amplitude;

\( A_{u1}, A_{u2}, A_{l1}, A_{l2} \) = upper1, upper2, lower1, lower2 carrier waves peak-to-peak amplitudes.

i. **Phase Disposition (PD):**

Gating signals for each phase are generated by comparing the sinusoidal waveform with four carrier waveforms [11]. There are four complimentary...
switch pairs in each phase. For a complimentary switch pair, turning on one of the switches excludes the other from being turned on. Using phase-a as an example, the four complementary pairs are (S1, S1’), (S2, S2’), (S3, S3’), and (S4, S4’). Gating signals S1’, S2’, S3’ and S4’ are generated by inverting S1, S2, S3 and S4, respectively [11]-[12]. Four carrier waveforms are in arranged as in phase. The converter is switched to +Vdc/2 when the sine wave is greater than both upper carrier. The converter is switched to +Vdc/4 when the sine wave is greater than first upper carrier. The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier. The converter is switched to -Vdc/4 when the sine wave is less than first lower carrier. The converter is switched to -Vdc/2 when the sine wave is less than both lower carriers [13].

The PD control scheme is represented in Fig. 2. The above formulas are applicable to sub harmonic PWM strategy i.e. PD, POD and APOD.

ii. Phase Opposition Disposition (POD):

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180° out of phase with carrier waveforms below zero reference. In this case, fundamental wave (50 Hz) and carrier wave with switching frequencies of 2 kHz are compared to generate switching pulses as shown in below fig. 3 [14].

![Carrier Wave](image1)

Fig. 2: SPWM PD Control Scheme

iii. Alternate Phase Opposition Disposition (POD):

Carriers are arranged in such a manner that each carrier is out of phase with its neighbour by 180 degrees [15] as shown in below fig. 4.

![Carrier Wave](image2)

Fig. 3: SPWM POD Control Scheme

B. Space Vector Pulse Width Modulation (SVPWM):

A well designed PWM strategy should have the following: 1) No pulse of opposite polarity in half cycle of line-line voltage waveform, 2) Sub harmonics should be zero, 3) It is always desirable to have one switch changing its conducting state at a time and 4) Do not allow different phase to switch simultaneously. In SPWM techniques we cannot ensure this all things. SVPWM is more general kind of approach than SPWM. In SVPWM, we can produce certain kind of waveforms that can not be produced by SPWM [4]. Compared to the SPWM, the SVPWM has a 15% higher utilization of the ratio. The biggest difference from other PWM methods is that SVPWM uses a vector as a reference. This gives the advantage of a better overview of the system. The reference vector is represented in a αβ-plane. The switches being ON or OFF are determined by the location of the reference vector in this αβ-plane [5]. The space vector pulse width modulation (SVPWM) technique offers significant performance benefits and has proved to be very popular in three-phase systems.

In a simple SVPWM method for multilevel three-phase topology presented [15], SVPWM involves synthesizing the reference voltage space vector by switching among the three nearest voltage space vectors [16]. SVPWM is considered better technique of PWM implementation, owing to its associated advantages as follows: 1) better fundamental output voltage, 2) better harmonic performance and 3) easier implementation in digital signal processor and microcontrollers. Fig. 6 illustrates the multicarrier SVPWM. For N-level diode-clamped inverter, this strategy arranges (N-1) triangular carriers with the same frequency and amplitude. The THD contents of Carrier SVPWM control scheme is shown in Fig. 10.

![Carrier Wave](image3)

Fig. 4: SPWM APOD Control Scheme

![Carrier Wave](image4)

Fig. 5: Multicarrier SVPWM
IV. SIMULATION RESULT

The diode clamped five level inverter is modelled in Simulink using power system block state. Switching signals for DCMLI are developed using Sinusoidal PWM and Space Vector PWM techniques discussed previously. Simulation model is performed by using different values of ‘m’ ranging from 0.6-1. Till modulation index (m)=1, inverter is under PWM control, above ‘1’ it goes into 6-step operation or a square wave mode. The moment it goes to square wave mode, the harmonics reappears. The frequency of predominant harmonics in square wave is again 5th, 7th and so on. The corresponding % THD values are measured by using FFT block and they are shown in TABLE 2. Fig. 1 shows the Matlab-Simulink model for five-level diode clamped multilevel inverter with PWM technique. It consists of 24 IGBT switches, 36 clamping diodes and 4 DC link capacitors are connected with single DC source. The Fig. 7 shows the overall line voltage waveform of three phase Five-level diode clamped multilevel inverter. THD values of five-level diode clamped multilevel inverter with PWM technique are shown in Fig. 8-9. THD values of different multicarrier PWM techniques are illustrated in Table: 2.

Table 3: THD analysis of control scheme with multicarrier techniques

<table>
<thead>
<tr>
<th>Control Scheme</th>
<th>Control Technique</th>
<th>% THD contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPWM</td>
<td>PD</td>
<td>20.22%</td>
</tr>
<tr>
<td></td>
<td>POD</td>
<td>21.80%</td>
</tr>
<tr>
<td></td>
<td>APOD</td>
<td>25.83%</td>
</tr>
<tr>
<td>SVPWM</td>
<td>PD</td>
<td>12.79%</td>
</tr>
<tr>
<td></td>
<td>POD</td>
<td>15.22%</td>
</tr>
<tr>
<td></td>
<td>APOD</td>
<td>15.37%</td>
</tr>
</tbody>
</table>

CONCLUSION

The comparative THD analysis of a three phase 5-level diode clamped multilevel inverter is presented in this paper. The various control schemes of multicarrier PWM technique like Phase disposition (PD), Phase opposition disposition (POD) and
Alternative phase opposition disposition (APOD) PWM techniques are applied to the proposed converter with sinusoidal wave (SPWM), third harmonic injection (THIPWM) and Carrier Space Vector (SVPWM). The THD values of the output voltages are compared with all the above mentioned techniques. From the above discussion, it is absorbed that the phase disposition Carrier SVPWM technique has less harmonic content in the output phase voltage compared with other multicarrier PWM control techniques and SVPWM is more general kind of approach than SPWM.

REFERENCES


