DESIGN OF PASS GATES ADDER CIRCUIT WITH IMPRROVED PERFORMANCE ON POWER CONSTRAINT

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Abstract- The main objective of this paper is to provide new lower power solutions for Very Large Scale Integration (VLSI) designs. Specially, this paper focuses on the reduction of the power consumption. In this paper, we have designed pass gate adder circuit by using different pass transistor logic like CPL (Complementary Pass Transistor Logic), DCVSPG (Differential Cascade Voltage Swing Pass Transistor Logic), SRPL (Swing Restore Pass Transistor Logic), EEPL (Energy Economized Pass Transistor Logic), Push – Pull Pass transistor Logic (PPL), and Single – Ended Pass Gate Logic (SEPG). The performance of this adder circuits are compared in terms of power consumption. These circuits are designed and stimulated using Microwind 3 software.

Keywords- Pass Gate Adder, Pass Transistor, Power Consumption,Microwind 3 software.

I. INTRODUCTION

A number of a different circuit design techniques are compared to find their efficiency in terms of power dissipation, delay & speed. The increasing demand for low-power VLSI (Very Large Scale Integration) can be addressed at different design levels, such as architectural, circuit layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinationalcircuits. This is because all the important parameters governing power dissipation, switchingcapacitance, transition activity, and short-circuit currents arestrongly influenced by the chosen logic style. Depending onthe application, the kind of circuit to be implemented, andthe design technique used, different performance aspectsbecome important, disallowing the formulation of universalrules for optimal logic styles. Power dissipation has becomea critical design metric for large number of VLSI circuits. The exploiting market of portable electronic appliancesfuels the demand for complex integrated system that can be powered by light weight batteries with larger recharge time. Therefore, in modern VLSI era the demand of low power design style becomes a hot research topic. This paper analyzes 16bit carry skip adder using pass transistor logic styles. These implementations are compared based on transistor count, power dissipation, and delay and power delay product. The power delivered in the output is one of the main factors to analyze the power dissipation of the circuit. The designed adder circuit has reduced the power dissipation due to CPL circuit implantation because it uses n-MOSFET. The propagation delay of our circuit has reduced tremendously than the reported results. The propagation delay, power dissipation and power delay product has obtained for different known sub-micron feature size.

II. NEED OF LOW POWER DISSIPATION

Power consumption is the main parameter in most of the electric appliances. The most obvious applications for which power consumption is critical are battery-powered applications, such as home thermostats and security systems, in which the battery must last for years.

High power dissipation leads to -
- High power dissipation increases time of operation
- High power dissipation require higher weight (batteries)
- High power dissipation reduces mobility.
- It needs high efforts for cooling.
- High power dissipation increases operational costs.
- High power dissipation reduces reliability.

Thus the low power dissipation will overcome all the above drawbacks. Low power also leads to smaller power supplies, less expensive batteries, and enables products to be powered by signal lines (such as fire alarm wires) lowering the cost of the end-product. As a result, low power consumption has become a key parameter of electronic circuits.

Need for Low power dissipation –
- Low power dissipation will reduce packaging costs.
- Low power dissipation will reduce chip and system cooling costs.
- Low power dissipation will increase noise immunity and system reliability.
- Low power dissipation will improve battery life (in portable systems)
- Environmental concerns.
- Growth of battery-powered systems.
- Users need for:

Mobility,
Portability

Reliability

 Low power dissipation will reduces total Cost.

 Low power dissipation will minimize environmental effects.

III. DESIGN METHODOLOGY

In this paper, we are designing a 16-bit non-clocked pass transistor carry skip adder(CSA) circuit by using different pass transistor logic like CPL, DCVSG, SRPG, EEPL&PPPL, which are the adder circuits very much useful in DSP energy executioncircuit. These adders are circuits are evaluated in terms of power dissipation, delay area, speed. The detail description of these pass transistors are given below.

1. Complementary Pass transistor Logic (CPL) - CPL uses series transistors to select between possible inverted output values of the logic, the output of which drives an inverter. The CMOS transmission gates consist of nMOS and pMOS transistor connected in parallel. Thefull adder circuit of complementary pass transistor logic (CPL) is shown in Fig(a) has swing restoration ability. The basic difference between the pass-transistor logic and the complementary CMOS logic is that the pass logic transistor network of the source side is connected with some input signals instead of the power lines. The advantage is that one pass- transistor network i.e. either PMOS or NMOS is sufficient to implement the logic function, which results in smaller number of transistors and input loads especially when NMOS network used. The output is a weak logic “1” when logic “1” is passed through a NMOS and a weak logic “0” when logic “0” is passed through a PMOS Therefore; output inverters are also used to ensure the drivability.

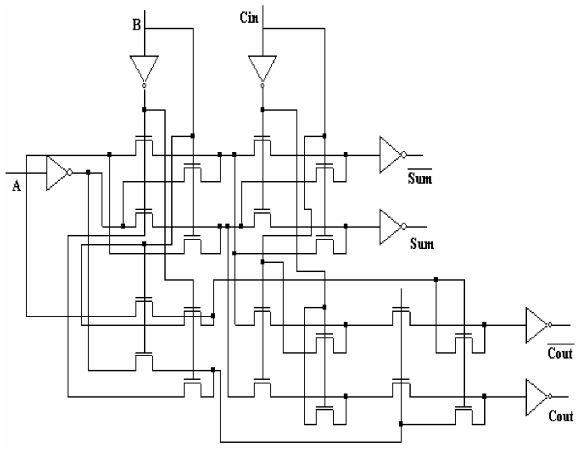

Fig.1(a) CPL

2.Single – Ended Pass Gate Logic (SEPG)-

The Single – Ended Pass Gate Logic (SEPG) are shown in fig.

(b). The specialized SEPG inverter is essentially a simple inverter with half-latched “keeper” PFET devices which brings the inverter input the restof the way up from VDD – VT to VDD.SEPG adder is used in a new trend of microprocessor circuit. SEPG concentrates on synthesizing the function of full logic blocks rather than individual logic functions. These SEPEGadder are performing fast and execute the bit without any signal loss. The Single – Ended Pass Gate Logic (SEPG),logic maintains logic flexibility in order to support general logic function solutions that do not necessarily resemble the standard Boolean solution. SEPG logic addressesassociated withimplementing pass gates logic in an automateddesign methodology.

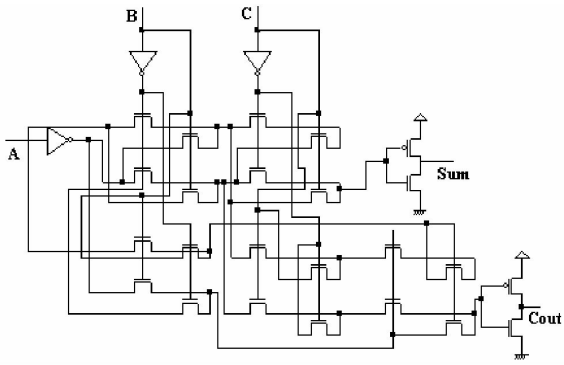

Fig.2 (b) SEPG

3. Differential Cascade Voltage Swing Pass Transistor Logic (DCVSPG)-

The meaning of DCVS logic with pass gate is that to extend the performancebenefits which associated with DCVSL into passgate topologies.By the implementing of pass gate topology, the DCVSPG logicperformancecan beextended. The DCVSPG requires two signals which are true and complementarysignals. Two complementary NFET switching trees are connected tocross-coupled PFET transistorsdepending on thedifferential inputs and whose one of the output is pulled down byNFET network. Then cross-coupled PFETtransistorslatchthe differential output. Since the inputsdrive only the NFET transistors of the switchingtrees. In DCVSPG, both the NFET and PFET contribute to pull upperformance, and both the outputs of true and complement are actively driven to their logical value.

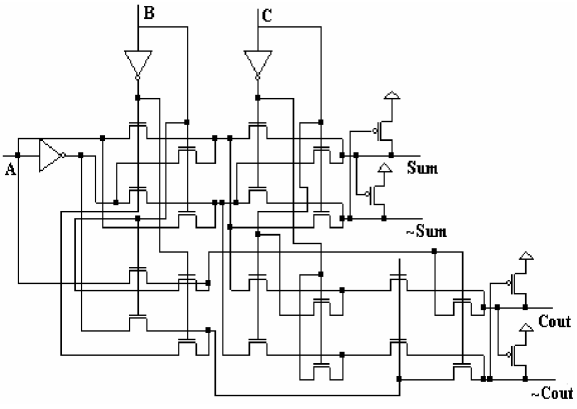

Fig.3(c) DCVS

4. Energy Economized Pass Transistor Logic (EEPL)-

EEPL is an Energy Economized Pass Transistor Logic, it reduce the power consumption and also reduce the delay in ancircuit operation by interrupting the feedback of latches which forming the load circuit in theStructure. The EEPL circuit action is simultaneously gives a regenerative positive feedback and also provides shorter delay than comparative CPL. Where the performance is still essential then EEPL will be a valuable logic elementfor a low power application. The circuit of Energy Economized Pass Transistor Logic is as shown in below fig.4(c).

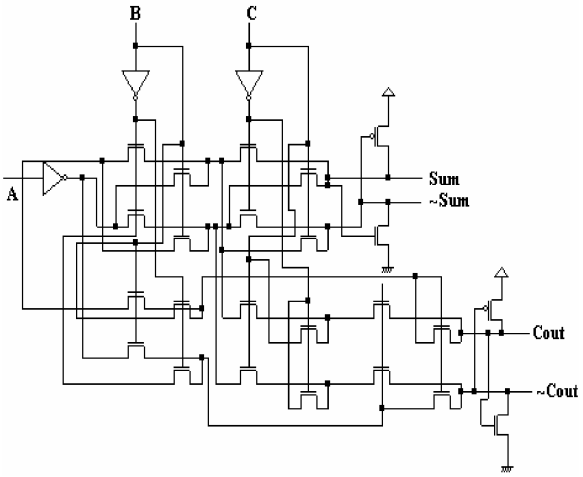

Fig.4 (d) EEPL

5. Push – Pull Passtransistor Logic (PPL) -

PPL is aPush – PullPass transistor Logic, it achieves a performance of advantage using complementary logic trees, and cross coupling to pull upor pull down devices . PPL recover the full rail voltage. In this operation of circuit, total device count, load circuitcapacitance, and power consumption is reduced. The Push – Pull Pass transistor Logic is a new innovation of recovering full VDD levels. The devices PFET and NFET connected at the load of the circuit is must include output node for getting the full rail voltage of output signal polarity. The circuit of Push – Pull Pass transistor Logic is as shown in an below fig.5(e).

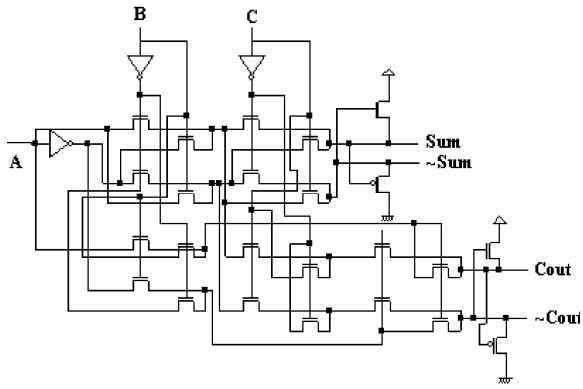

Fig.5(e) PPPL

IV. RESULT AND DISCUSSION

The 5 types of pass gate adder circuit have been designed and verified using CAD tools of DSCH 3. The circuit has been simulated by the microwind 3.1.The 5 types of pass gate adder circuits are designed & these circuits are verified using Truth table (1). The power dissipation is determined for various adder circuits of feature size of 0.35 µm, 0.25µm, provides less power dissipation & high performance speed in technology 0.18µm, 0.25µm,0.35µm than the other adder logic circuits.We have also compared oursimulated results with the reference paper [3] published results and observed better performance in terms of power dissipation.0.18µm.our simulation result is shown in table (2). The truth table is shown in table 2. The significance of our project is that we have got lowest power dissipation. At feature size of 0.18 µm, the power dissipation in PPPL is lowest among all the five adder circuits.

Input			Output	
A	B	Cin	Sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table (1) Truth table

Feature size In µm	Variable	CPL	DCVS	EEPL	PPPL	SEPG
0.34 µm	Power dissipation (in mW)	1.073	0.945	1.743	0.779	0.890
	No. of transistors	34	28	30	30	30
0.25 µm	Power dissipation (in mW)	0.601	0.467	0.819	0.417	0.449
	No. of transistors	34	28	30	30	30
0.18 µm	Power dissipation (in mW)	0.279	0.249	0.437	0.226	0.241
	No. of transistors	34	28	30	30	30

Table (2) Simulation Result for Power Dissipation

CONCLUSION

We have designed different pass transistor adder logic with for low power and high performance of multiplier circuit. We have analyzed power dissipation and number of transistors which are calculated from the simulation results. We have analyzed the simulated results and found that PPPL circuit.

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