DESIGN OF SPEED AND POWER EFFICIENT 64X64 BIT URDHVA TIRYAKBYHAM MULTIPLIER

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Abstract: Multipliers are one of the most widely used digital component in the digital integrated circuit design and are the necessary part of many digital signal processing applications such as correlations, convolution, filtering, frequency analysis, image processing etc. with advances in technology, researchers have tried and are trying to design multipliers which offer either high speed, low power consumption, less area or combination of them. This paper focus on the development of high speed low power multiplier using Vedic mathematics. The proposed 64X64 bit multiplier architecture is designed using modified full adder carry save adder and it achieves 60% improvement in speed and 37% improvement in power as compared with that of conventional array multipliers.

Keyword- Vedic Mathematics, Urdhva tiryakbyham, Carry save adder.

I. INTRODUCTION

Multiplication process is used in many applications like Instrumentation and Measurement, Communications, Audio and Video processing, Image Enhancement, Navigation, Radar, Global Positioning System (GPS), control applications like Robotics and Machine Vision, etc. Multipliers are the key components of many high performance systems such as FIR filters, Microprocessors and Digital Signal Processors (DSP).

A typical processor will consume a considerable amount of time in performing the arithmetic operations, particularly the multiplication operation. The system performance is generally determined by the performance of the multipliers. Hence, there is a need for highly efficient and sophisticated multiplier.

The need of fast multiplication gives rise to algorithm such as baugh-wooley method, booth multiplier using recoding bits, modified booth algorithm (MBE), although the MBE is most successful algorithms yet it is also a time consuming process .Nowadays, new methods are required for even faster multiplication, the conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics.

Vedic mathematics is a gift given to this world by ancient sages of India. Vedic mathematics is an extract from the four Vedas (Books of Wisdom). Owing to its simplicity and regularity it finds its utility and applications in the field of geometry, trigonometry, quadratic equations factorization and calculus. The word ‘Vedic’ is derived from the word ‘Veda’, which means store house of all knowledge. Vedic formulae are claimed to be based on “the natural principles of which the human mind works”.

II. VEDIC MATHEMATICS

Vedic mathematics are rediscovered by Jagadguru Swami Sri Bharati Krishna Tirthaji (1884-1960), a scholar of Sanskrit, Mathematics, and History of philosophy. The whole mathematics is based on 16 sutras (Formulæ) and 13 upa sutras (Sub Formulæ). The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. This is so because the Vedic formulæ are claimed to be based on the natural principles on which the human mind works. The most striking feature of the Vedic system is its coherence. Instead of a hotchpotch of unrelated techniques the whole system is beautifully interrelated and unified.

Multipliers based on the Urdhva Tiryakbyham sutra of Vedic mathematics are more efficient than the conventional array multiplier [4] [5].

A. Urdhva-Tiryakbyham Sutra

The Urdhva - Tiryakbyham sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done and then the concurrent addition of these partial products can be done. This parallelism in generation of partial products and their summation is obtained using Urdhva-Tiryakbyham [3]. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessor to operate at increasingly high clock frequencies, which in turn reduces the power dissipation.
64-bit urdhva multiplier has been developed in a hierarchical manner. Fundamental block of developed multiplier is 2-bit multipliers.

B. Multiplication using Urdhva sutra

The hardware realization of 2-bit multiplier requires four two input AND gates and two half adders.

![Fig:1 hardware implementation of 2-bit urdhva multiplier]

III. PROPOSED MULTIPLIER ARCHITECTURE

The proposed multiplier architecture mainly consists of following:

- Design and implementation of modified power efficient full adder architecture.
- Design higher order adders by using the modified full adder architecture, finally these adders are used in proposed Vedic multiplier architecture in order to improve power and speed.

A. The Modified Full Add

Normal full adder consists of XOR, OR and AND gates consumes more power because XOR gate itself will consume more power. The modified full adder structure consists of NAND, OR and AND gates and it reduces the power consumption. Also the carry generation is faster in this [1]. If such design is used in the multiplier architecture then power can be reduced considerably and also it increases the speed.

![Figure 2: Modified Full Adder]

B. 64×64 bit proposed Urdhva multiplier

The 2-bit multiplier is used to develop other hierarchical blocks such as 4-bit, 8-bit, 16-bit and 32-bit multipliers respectively. The 64-bit multiplier requires four 32-bit multipliers and three carry save adders. Partial product generated by each block of the multiplier is given to the adder blocks. First 32-bits of the first multiplier give the final 32-bits of the product and the remaining 96-bits are the output of the carry save adder.

![Figure 3: Hardware Realization of 64-Bit Vedic Multiplier]

IV. RESULTS AND COMPARISONS

The proposed multiplier architectures using Vedic mathematics have been coded using Verilog HDL and the simulations are carried out using Xilinx ISE 13.1 version.

![Figure 4: Simulation result of modified full adder]
Figure 5: Synthesize circuit for modified Full adder

Table 1: Power Comparison between Normal and Modified Full adder

<table>
<thead>
<tr>
<th>Instances</th>
<th>Leakage Power (nw)</th>
<th>Dynamic Power (nw)</th>
<th>Total Power (nw)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Full Adder</td>
<td>0.038</td>
<td>549.416</td>
<td>549.454</td>
</tr>
<tr>
<td>Modified Full Adder</td>
<td>0.031</td>
<td>446.941</td>
<td>446.973</td>
</tr>
</tbody>
</table>

From the above report, it can be concluded that the normal full adder consumes the total power of 549.454 nw and requires 1 cell area. Modified full adder consumes 446.973 nw and requires 3 cells area. So with the use of modified full adder one can achieve 18% improvement in power.

A. Simulation Result of proposed 64X64 bit Urdhva Multiplier

The simulation result for 64-bit Urdhva multiplier is shown in figure 6. Here ‘a’ and ‘b’ is the inputs to the multiplier, both are of 64-bit width and ‘q’ is the output of the multiplier which is about 128-bit width. When a =ffffffffffffffff and b = ffffffffffffffff, it produces the output as ffffffff80000000000000001

Figure 6: Simulation result of proposed 64X64bit Urdhva multiplier

B. Power and Speed Comparison of Conventional and Vedic Multipliers

<table>
<thead>
<tr>
<th></th>
<th>Leakeage power(nw)</th>
<th>Dynamic power(nw)</th>
<th>Total power(nw)</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 bit array multiplier</td>
<td>172.668</td>
<td>13.763</td>
<td>13.763</td>
</tr>
<tr>
<td>64 bit Urdhva multiplier with normal full adder</td>
<td>306.020</td>
<td>9.219</td>
<td>9.220</td>
</tr>
<tr>
<td>64 bit Urdhva multiplier with modified full adder</td>
<td>286.782</td>
<td>8.609</td>
<td>8.609</td>
</tr>
</tbody>
</table>

Table 2: Speed Comparison of 64-Bit Array and Urdhva multiplier

<table>
<thead>
<tr>
<th></th>
<th>Array Multiplier</th>
<th>Urdhva Multiplier</th>
</tr>
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<tbody>
<tr>
<td>Frequency(MHz)</td>
<td>5.5</td>
<td>13.9</td>
</tr>
</tbody>
</table>

Table 3: Power Comparison of 64-Bit Array, Urdhva multiplier with normal full adder and Urdhva multiplier with modified full adder

V. SCOPE FOR FUTURE DIRECTIONS

1. The methodology proposed for Vedic multipliers have been implemented at gate level. This can be further improved upon by using power optimization techniques such as RTL Clock gating, Dynamic Voltage Frequency Scaling (DVFS), Power gating etc. at the transistor level.
2. The speed of Vedic multiplier can further be increased by adopting pipelining and parallelism concepts.
3. Vedic multipliers are very much suitable for low power applications, hence can be utilized in floating point units which are power hungry designs.

CONCLUSION

The proposed multiplier architecture is based on the urdhva sutra of the Vedic mathematics. Here power efficient, higher order adders are designed using modified full adder. These adders are used in proposed 64 bit Vedic multiplier architecture which proved 60% improvement in speed and 37% improvement in power as compared with that of existing conventional array multiplier architecture.
REFERENCES


