IMPLEMENTATION OF HIGH SPEED ENHANCED CSLA BASED ON GATED D-LATCH

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Abstract- Adder plays an important role in any part of the computational systems like addition, subtractions, high speed multiplications, DSPs and ALUs. There are several types of adders like Parallel Adder, Ripple-Carry Adder (RCA), Carry Look-Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSLA) etc. Each adder has its own performance in reducing parameters like area, delay and power. From the structure of CSLA, there is a scope of modifying circuit in turn which increases the speed. Speed is one among the various VLSI parameters which is dealt in this project “Implementation of High Speed Enhanced CSLA Based on Gated D-Latch”. Carry Select Adder is the fast adder used for fast arithmetic functions in the data processors compared to other conventional adders. Gated D-Latch was replaced instead of RCA with carry-in as ‘1’ in Regular CSLA (RCSLA) and BEC in Modified CSLA (MCSLA). In this project 16-bit, 32-bit and 64-bit Enhanced CSLA (ECSLA) have been developed and had better out comes compared with RCSLA and MCSLA. Thus if we compare with MCSLA the proposed system ECSLA is about 52.753% faster and 34.993% faster than RCSLA. The project was simulated and synthesized using Xilinx ISE Design Suite 14.4 and implemented on Xilinx-Spartan 3E-FPGA kit.

Keywords - Enhanced CSLA (ECSLA), Gated D-Latch, Modified CSLA (MCSLA), Regular CSLA (RCSLA), Xilinx ISE Design Suite 14.4.

I. INTRODUCTION

In any digital system addition is the fundamental operation. An adder can perform arithmetic operations such as subtraction and logical operations like AND, XOR, XNOR and OR etc. As these adders have the ability to produce those operations it is essential to have a high speed adder. In digital adders, the speed of addition is given by the time taken to forward a carry through the adder. The sum for each bit in an elementary adder is produced sequentially only after the previous bit place was added and a carry is forwarded into the next place.

In the past few years, several adders have been proposed by many members. The carry propagation delay problem which is overcome by independently generating multiple radix carriers, using this carries simultaneously generated sums were selected, which is proposed by O. J. Bedriji. A new scheme is introduced by Akhilash Tyagi to generate carry bits with block carry in ‘1’ from the carries of a block with block carry in ‘0’. T. Y. Chang and M. J. Hsiao proposed add one circuit to replace one RCA instead of using dual RCA in a CSLA scheme. A modified CSLA designed in different stages which reduces the area was proposed by Padma Devi et al. An area efficient VARIABLE CSLA scheme was proposed by Yajuan He et al To reduce the maximum delay the carry is forwarded in to the final stage of Carry Save Adder, Ramkumar et al proposed a Binary to Excess-1 Converter (BEC) method. The basic idea of this work is to use Gated D-Latch instead of RCA with carry in 1 in RCSLA and BEC in MCSLA. The main benefit of Gated D-Latch is to reduce the delay and achieve high speed CSLA. The details of Gated D-Latch are discussed in Section II. Implementation of ECSLA is discussed in Section III. Simulation results and RTL Schematic diagrams are shown in Section IV. Finally the work is concluded in Section V.

II. GATED D-LATCH:

Latches and Flip Flops are the fundamental building blocks of digital electronic systems used in communications, computers and many other systems. Latches are used as data storage elements. A latch is a circuit having two stable states (current state-Q, compliment of current state-Q'). A latch is a Level-Sensitive, where as flip-flops Edge-Sensitive. When a latch is enabled it becomes transparent.

![Fig.1: Circuit diagram of Gated D-Latch.](image1)

![Fig.2: Logic Symbol of Gated D-Latch.](image2)
combinations, which is also known as transparent latch, data latch or gated latch. It has a data input-D and an enable signal-En (we can also use a clock or control signal) as inputs and two stable output states Q and Q'. The word transparent was obtained as the signal propagates directly through the circuit from input-D to the output-Q when the enable input is ON. When enable input is OFF there will be no change. The Logic Symbol of Gated D-Latch is shown in fig.2 and truth table is shown in table1.

<table>
<thead>
<tr>
<th>En/C</th>
<th>D</th>
<th>Q</th>
<th>Q’</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>Q_{previous}</td>
<td>Q’_{previous}</td>
<td>No Change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Reset</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Set</td>
</tr>
</tbody>
</table>

III. IMPLEMENTATION OF ENHANCED CSLA BASED ON GATED D-LATCH:

The implementation of 64-bit enhanced CSLA based on Gated D-Latch is shown in fig 3. The design was constructed in hierarchical model (top-down design). The 64-bit is divided into two 32-bits and again each 32-bit is divided into two 16 bits.

The inputs A, B and En are applied. RCA performs two additions as En is a clock signal we get both Logic ‘0’ and Logic ‘1’. When En is considered as Logic ‘1’ then the RCA performs addition, the obtain Sum from the RCA acts as input to the Gated D-Latch. As discussed before about Gated D-Latch when enable signal is high the output of the Gated D-latch will be same as the input.

When En is considered as Logic ‘0’ then RCA performs addition, the obtain Sum in the RCA will be stored in it only. Now based on the previous block carry the output is selected as either a Gated D-Latch output (when carry= '1') or RCA output (when carry= '0') through the 2:1 mux.

The 16-bit design present in fig 3 is as shown in fig 4; it is again divided into different groups of variable sizes. Each block has some bit length of different sizes. Each block consists of a Ripple Carry Adder (RCA), Gated D-Latch and a multiplexer to each block excluding the block 0, because it is having only one RCA corresponding to that block, so to select the data there is no need of multiplexer.
Fig 5 shows the internal structure of block0 of fig 4. It is a 2-bit RCA which contains a series of two full adders in cascade form.

Fig 6: Internal Structure of Block1 of fig 4.

Fig 6 shows the internal structure of block1 of fig 4. It is also a 2-bit RCA which contains a series of two full adders in cascade form and three Gated D-Latches with enable signal En.

Fig 7: Internal Structure of Block2 of fig 4.

As shown in fig 7 Internal Structure of Block2 of fig 4 contains 3 full adders and 4 Gated D-Latches and 4 multiplexers to select 3-bit SUM and a Carry out to that particular block.

As shown in fig 8 Internal Structure of Block3 of fig 4 contains 4 full adders and 5 Gated D-Latches and 5 multiplexers to select 4-bit SUM and a Carry out to that particular block.

Fig 8: Internal Structure of Block3 of fig 4.

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Fig 9: Internal Structure of Block4 of fig 4.

As shown in fig 9 Internal Structure of Block4 of fig 4 contains 5 full adders and 6 Gated D-Latches and 6 multiplexers to select 5-bit SUM and a Carry out to that particular block. Finally we obtained a 16-bit SUM and a Carry out. Where as for 16-bit RCSLA the design is as shown in fig 10. This contains two RCA’s and a multiplexer in each block excluding the block 0, because it is having only one RCA corresponding to that block, as we need not select the data there is no need of multiplexer.

As shown in fig 9 Internal Structure of Block4 of fig 4 contains 5 full adders and 6 Gated D-Latches and 6 multiplexers to select 5-bit SUM and a Carry out to that particular block. Finally we obtained a 16-bit SUM and a Carry out. Where as for 16-bit RCSLA the design is as shown in fig 10. This contains two RCA’s and a multiplexer in each block excluding the block 0, because it is having only one RCA corresponding to that block, as we need not select the data there is no need of multiplexer.

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Where as for 16-bit MCSLA the design is as shown in fig 11. This contains RCA, BEC and a multiplexer in each block excluding the block 0, because it is having only one RCA corresponding to that block, as we need not select the data there is no need of multiplexer.
IV. EXPERIMENTAL RESULTS

4.1 Simulation Results:
The simulation process has been carried out for different levels of abstraction. The simulation has been extended up to our requirement i.e. 64-bit. The code has been written in Verilog hardware description language.

The top module has been synthesized and simulated in Xilinx ISE Design Suite 14.4 and the corresponding delay calculations have been noted. By using Gated D-Latch the delay was reduced.

Simulation results are shown in fig 12, 13, 14 for 16-bit, 32-bit and 64-bit. RTL Schematic diagrams are shown in fig 15, 16, 17 for 16-bit, 32-bit and 64-bit. The design was implemented in Spartan-3E kit.

4.2: RTL (Register Transfer Level) schematic diagrams:
CONCLUSION

This paper has really given an effective description on implementation of high speed Gated D-Latch based Enhanced Carry Select Adder (ECSLA). This has been achieved by replacing RCA with carry in “1”, by Gated D-Latch which intern helped us to have a new advantageous ECSLA adder than previous adders like RCSLA and MCSLA. Replacing RCA with Gated D-Latch the propagation delay was reduced. The applications of Enhanced Carry Select Adder are used in many electronic applications like calculators, arithmetic logic unit(s) used in processors (like DSP’s), computers and are also used where the table indices, addresses are to be calculated faster and where more number of bits are to be added using complex adders for signed number representations.

FUTURE SCOPE

Future scope of this project is, new types of adders can be developed in place of RCA and there by the area and delay of the adders can be decreased as the number of bits increases simultaneously.

BIBLIOGRAPHY


Table V. Comparison Table for Regular, Modified & Enhanced CSLA:

<table>
<thead>
<tr>
<th>No. Of Bits</th>
<th>Regular CSLA</th>
<th>Modified CSLA</th>
<th>Enhanced CSLA</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-Bit</td>
<td>16.204</td>
<td>16.634</td>
<td>14.328</td>
</tr>
<tr>
<td>32-Bit</td>
<td>18.257</td>
<td>24.790</td>
<td>18.056</td>
</tr>
<tr>
<td>64-Bit</td>
<td>31.535</td>
<td>43.389</td>
<td>20.500</td>
</tr>
</tbody>
</table>