DESIGN AND SIMULATION OF VERNIER RING OSCILLATOR TDC WITH IMPROVED RESOLUTION

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Abstract - TDC plays a very important role in most of the high energy nuclear physics time of flight experiment for achieving high resolution. The traditional time interval experiment measurement totally depend on such kind of methods like Time-to-Amplitude Conversion, Vernier method, Delay Locked Loops (DLL), Tapped Delay Lines (TDL), Differential Delay Lines (DDL), current -Integration TDC, & Counter-Based TDC etc. Many time-of-flight (TOF) applications required measurement of the time intervals between two events. Time to digital converter is becoming more suitable for these kinds of applications because it measures the time difference between two pulses and gives time difference as a digital output code. However, basic TDC needs much higher clock frequency to measure smaller time intervals between two events in terms of picoseconds. The main advantage of migrating TDC in the FPGA paradigm is making the best of its configuration and reconfiguration capabilities. The resolution below the minimum gate delay is achieved by employing Vernier oscillator technique. We present here a high resolution TDC based on vernier ring oscillator principle of nearly 70ps resolution.

Keywords - TOF, Time to Digital Converter, Vernier Delay Line, Field Programmable Gate Array, Ring Oscillator.

I. INTRODUCTION

Time to Digital Converter is widely used in electronic to convert time to digital code. Originally it is developed for nuclear experiments to locate single-shot events; recently, it has been employed to measure phase in all-digital phase-locked loops (PLL) [3]. The TDC is now being used in many applications such as space science instruments, physical instruments, high energy particle detectors phase meters, and digital storage oscilloscopes, laser range finders, and measurement devices. Precise measurements of time interval are performed with the use of various methods in both the analog and digital domains. The digital methods become predominant due to the ease of implementation in integrated circuits, shorter conversion time, and higher immunity to external disturbances. In all these applications the adoption of the Vernier method permits achieving sub-gate delay time resolution.

First, a physical quantity is converted to a time signal and then digitized by a time-to-digital converter (TDC) to get them corresponding digital output. It measures the time interval between two events. The time intervals between two rising edges or two electrical timing signals, also called start and stop signals, will be quantized and then converted into digital data [2].

A combination of a counter and interpolation has been proposed for a large linear dynamic range and high resolution TDC (Nutt 1968, Kalisz 2004). The counter keeps track of the full clock cycles elapsed since the arrival of the start pulse. The counter is either halted with the stop pulse or the stop pulse stores the state of the counter [2].

II. VERNIER RING OSCILLATOR TDC

The significant blocks of the TDC are ring oscillators, phase detector, and fast counters. The two ring oscillators with a slight difference in the period are obtained as shown in Fig.3. The oscillator design combines features like trigger synchronized starting & stopping and retrigger-ability. The very small and precise difference in periods is achieved by carefully evaluating the place & route delays in both oscillator circuits and by changing the feedback load [7] as shown in Fig.3. In this project, the slow oscillator’s And-Or-Invert gate has a fan-in of two and larger delay, whereas the fast oscillator’s NOR gate has a fan-in of one and minor delay. This generates a slight difference in periods. Two long duration counters exercised in calibration determines the exact difference in periods and calibrates the TDC. Here, T2 < T1 and STOP pulse will come after START pulse, at some point the rising edge of the fast clock will coincide with the rising edge of the slow clock, which will recognize by a phase detector. Circuit for phase detector is given in fig.3 In the FPGA based implementation. There are two oscillators produce signals of frequencies $f_1 = 1/T$ and $f_2 = 1/T_2$ differing only slightly

The incremental resolution is presented by the difference between T1 and T2, given by
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$$R = T_{\text{slow}} - T_{\text{fast}}$$

Signal and the phase difference between these two signals is smaller than the required setup time.

### III. PROPOSED DESIGN

The proposed design of Vernier Ring Oscillator TDC is the VTDC that utilizes two triggerable oscillators with a precise oscillation frequency difference to replace the VDL in the conventional VTDC. The phase detector keeps track of the history of the phase difference between two oscillators and stops the measurement process once $T_1$ begins to lead $T_2$. On the first rising $T_1$ edge after the rising edge of $T_2$, the output of the first register $Q_1$ goes high. On the following rising edge of $T_2$, the second register keeps the value of $Q_1$ and switches $Q_2$ to high. When the signal edge of $T_1$ catches up with $T_2$, the output $QD_1$ rises and switches the output of the AND gate to generate the Phase Detected signal, as shown in Figure 3. The Phase Detected signal is fed to the counter where it stops the time measurement process.

Resolution is the difference of slow clock and fast clock, and the meta-stability is likely to happen in the phase detector, when the $T_1$ signal catches up with $T_2$. The resolution is the time difference between slow oscillator time period and fast oscillator time period, and it is defined by:

$$\text{Resolution} = T_{\text{slow}} - T_{\text{fast}}$$

$$T_{\text{in}} = (n_1 - 1) T_1 - (n_2 - 1) T_2$$

$$= (n_1 - n_2) T_1 + (n_2 - 1) R$$

When $T_{\text{in}} < T_{\text{slow}}$, then $n_1 = n_2$ and $T_m$ is given by:

$$T_{\text{in}} = (n_2 - 1) R$$

Where,

- $T_1$ = Time period of slow oscillator
- $T_2$ = Time period of fast oscillator
- $n_1$ = Counted number of slow clock
- $n_2$ = Counted number of fast clock

Resolution of the system = $T_1 - T_2$

### IV. SIMULATIONS AND RESULTS

The simulations are performed using ISE Xilinx software.

- Fig. 7: Output waveform of slow oscillator
- Fig. 8: Output waveform of Fast oscillator
The result of start & stop clock is given above fig.7 & Fig.8.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow oscillator period (T1)</td>
<td>20.270ns</td>
</tr>
<tr>
<td>Fast oscillator period (T2)</td>
<td>20.200ns</td>
</tr>
<tr>
<td>Resolution $\Delta t = T_1 - T_2$</td>
<td>70ps</td>
</tr>
</tbody>
</table>

Table I: TABULATED VALUES OF THE TEST RESULTS

<table>
<thead>
<tr>
<th></th>
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<tbody>
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<td>Time Resolution (ps)</td>
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<td>200ps</td>
<td>160ps</td>
<td>70ps</td>
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<td>Structure</td>
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<td>Vernier</td>
<td>Vernier Ring Oscillator</td>
<td>Vernier Ring Oscillator</td>
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<tr>
<td>Device</td>
<td>FPGA</td>
<td>FPGA</td>
<td>FPGA</td>
<td>FPGA</td>
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Table II: COMPARISON OF RESULTS OF PROPOSED DESIGN WITH EARLIER DESIGN

V. CONCLUSIONS

It is hard to get TDC with few picoseconds resolution in FPGA paradigm. The purpose of this work was to develop a time-to-digital converter architecture with a fine and coarse counter achieved high resolution, low power consumption, small area and low cost. This paper reports optimization of area as well as reduce the floor planning burden. Hence it is an area efficient TDC useful for the application mentioned in [10]. Our Vernier techniques resort to maintain stable resolution of 70ps. Vernier delay ring architecture is folded back to its beginning to increase the dynamic range without adding more delay elements and also achieves low power consumption.

REFERENCES