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DESIGN OF N-BIT TREE BASED COMPARATOR

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Abstract - Reversible logic gates gain attention in recent years due to its low power consumption ability. It is used in advance computing, DNA computing, quantum computation, low power CMOS design and nanotechnology. In this paper an n-bit optimized tree based reversible comparator is proposed using existing reversible logic gates. The design is realized and the parameters garbage output, Ancilla/constant input, quantum cost and delay are calculated. The design is simulated using ISE simulator (Xilinx 14.7, spartan 6).

Keyword - Reversible Gate, Quantum Cost, Ancilla Input, Garbage Output, Comparator.

I. INTRODUCTION

Conventional digital circuits are designed using basic logic gates which dissipate heat for each bit of information loss. [1]R. Landauer shows KTln2 joules (K is Boltzman's constant, T is operating Temperature) of energy is dissipated per bit of information loss. Bennett [2] showed that the information loss can be avoided using Reversible logic circuits.

Reversible Logic Gate: Circuit is said to be reversible if number of input is equal to number of output and there is an one-to-one correspondence between input and output. In reversible logic gates input can be recovered from output, in addition to deducing output from input.

Ancilla Input (AI): Inputs to reversible gate that are maintained constant at 0 or 1 to deduce the logical function.

Garbage Output (GO): Outputs that are not useful but exists just to achieve reversibility. Relation between number of Constant input and Garbage output is given below

$$Inputs + constantInput = Output + GarbageOuput \quad \text{....[3]}$$

Delay: Minimum gate count in the path between input to output.

Quantum Cost (QC): Cost of circuit in terms of primitive gate.

In this paper 8-bit reversible tree based comparator is proposed. The paper is organized in to sections. Section 2 contains the description of basic reversible logic gate along with their block diagram and symbols, that are used in the proposed design. The proposed design of the comparator is explained in section 3, section 4 give the parameter comparison of proposed design with other existing researches. Finally the paper is concluded in section 6.

II. REVERSIBLE GATES

The basic reversible gates that are used in the proposed model are Feynman, Toffoli, Peres and BJS gates, details of these gates are provided below.

A. NOT gate

NOT is a 1×1 reversible gate. Symbol of NOT gate are shown in Fig 1. QC of NOT gate is 1 and delay is 1Δ.

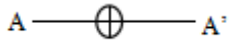

Figure 1. Symbol of NOT gate

B. Feynman gate (FG)

Feynman gate is also known as CNOT (Controlled NOT) gate [5], is a 2×2 reversible gate. Symbol and block diagram of Feynman gate are shown in Fig 2. QC of FG is 1 and delay is 1Δ.

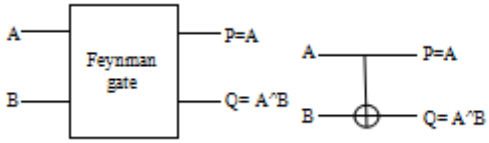

Figure 2. Feynman gate

C. Toffoli Gate (TG)

Toffoli is a 3×3 reversible gate, also known as C^2NOT (controlled-controlled NOT) gate [3]. Symbol and block diagram of Toffoli gate are shown in Fig 3. QC of TG is 5 and delay is 5Δ.

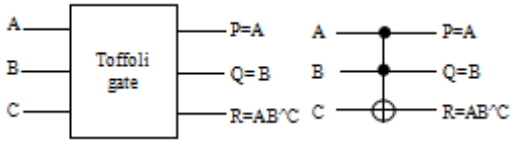

Figure 3. Toffoli gate

D. Peres Gate (PG)

Peres is a 3×3 reversible gate [4]. Symbol and block diagram of Peres gate are shown in Fig 4. QC of PG is 4 and delay is 4Δ.

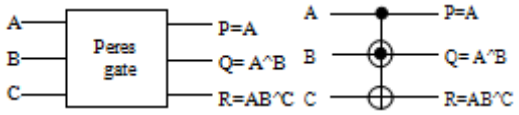

Figure 4. Peres gate

E. BJS Gate

BJS gate is a 4×4 reversible gate. Symbol and block diagram of BJS gate are shown in Fig 5. QC of BJS gate is 6 and delay is 6Δ.

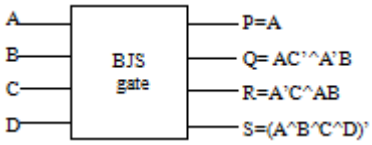

Figure 5. BJS gate.

III. PROPOSED COMPARATOR DESIGN

1-bit comparator is designed using BJS gate. BJS gate can be used as one bit comparator by making its B and D input as zero, so that the output Q is AB' which is A greater than B, R is A'B i.e, A less than B and S is (A^B)' which is A equal to B result.
Figure 6. shows the implementation of 1-bit comparator using BJS gate, whose quantum cost is 6.

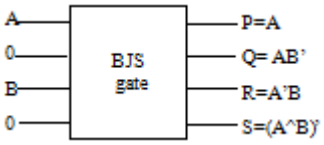

Figure 6. 1-bit comparator using BJS gate

Further 2-bit comparator can be designed using BJS gate with Toffoli and Peres gate. The output of 2 BJS gate (n and n-1 bit) that contains the result of single bit comparison is passed through the toffili and peres gate that produce the result of 2-bit comparison. Quantum cost of proposed 2-bit comparator is 21, which is calculated considering the QC of BJS, Toffoli and Peres gate shown in below equation.

$$QC_{2bit_{comparator}} = 2 \times QC_{BJS_{gate}} + QC_{Toffoli\_gate} + QC_{Peres_{gate}}$$

$$QC_{2bit\ comparator} = 2 \times 6 + 5 + 4$$

and the delay is 15 (Delay of BJS + Delay of Toffoli + Delay of Peres).

Figure 7. shows the implementation of proposed 2-bit comparator circuit.

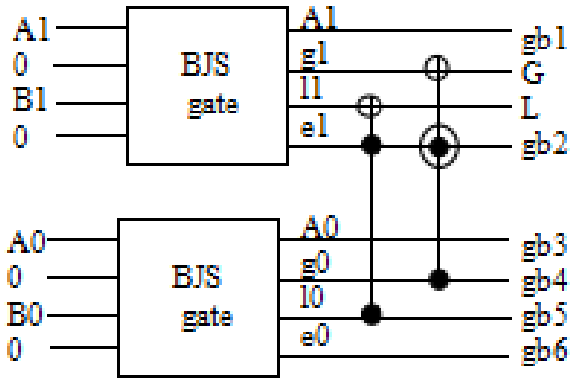

Figure 7. proposed 2-bit comparator

The circuit only produce greater and lesser output signal, to deduce equal the output of the above circuit is given to the proposed output circuit (POC) which produced all the three signal greater, lesser and equal.

Figure 8. shows the implementation of POC circuit, which is designed using two Feynman gate. QC of POC circuit is 2.

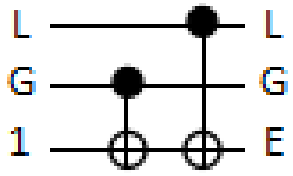

Figure 8. POC circuit

The 4-bit comparator is designed using the proposed 2-bit comparator connected in tree model, output of the fist stage proposed 2-bit comparator is given to the proposed 2-bit comparator of stage-2 which produce greater and lesser signal then this output is given to POC circuit to deduce all the three output signal.Figure 9. shows the design of 4-bit comparator circuit.

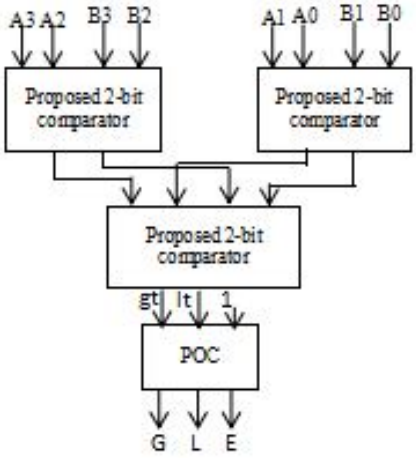

Figure 9. 4-bit comparator

QC of the 4-bit comparator circuit is 65 and the delay is 32.

Figure 10. shows the implementation of 8 bit comparator design

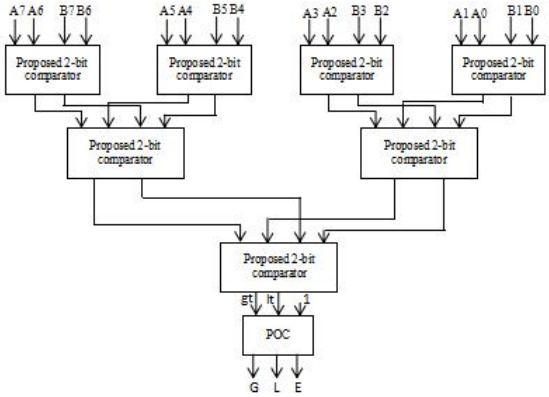

Figure 10. 8-bit comparator

The quantum cost , number of ancilla inputs, garbage output, number of gates used in design and delay are given in below table

Bits	8	16	32	64	N-bit
QC	149	317	653	1325	21n-19
AI	29	61	125	253	4n-3
GO	42	90	186	378	6n-6
GC	30	62	126	254	4n-2
Delay	47	62	77	92	15logn+2

Table 1. Parameter for n-bit comparator

IV. COMPARISON RESULT

The comparison of Quantum cost, Ancilla input, Garbage output, Gate count and delay of existing design and the proposed design are given in table 2.

Design	[7]	[6]	[8]	[9]	[13]	[14]	Proposed
Bits	4	8	4	4	8	8	8
QC	134	135 198	52	unknown	140	185	149
AI	10	29	11	4	23	29	29
GO	15	42	15	8	36	42	42
GC	18	68	20	10	67	72	30
Delay	36	61	19	unknown	unknown	57	47

Table 2. Comparison of Proposed design with existing design

Percentage of improvement of proposed design with respect to either QC, delay or GC from the existing ones is shown in Table 3.

Design	QC	AI	GO	GC	Delay
[6]	135 198	29	42	68	61
[13]	140	23	36	67	unknown
[14]	185	29	42	72	57
proposed	149	29	42	30	47
% improvement with [6]	24	0	0	55.8	22.9
% improvement with [13]	-6	0	-16	55.2	-
% improvement with [14]	19	0	0	59	19

Table 3. Comparison results for % improvement of proposed design

CONCLUSION

In this paper an optimized reversible tree based comparator is proposed. Various parameter such as quantum cost,gate count and delay are optimized. The design uses minimum number of gates and thus reduces the gate count by about 50%. The comparator can be extended to compare N-bits by increasing the 2-bit comparator and stages of comparison.

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