A SURVEY ON POWER OPTIMIZATION OF 8-BIT MAGNITUDE COMPARATOR USING PRE-COMPUTATION AND BINARY DECISION DIAGRAM

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Abstract - Power optimization is the primary constraint in recent technologies.Due to transistor scaling,clock frequency and chip transistor count,power dissipation increases.The need of low power design is a major concern in high performance digital systems.This can be achieved by using Binary Decision Diagram (BDD) and pre-computation logic.Symbolic model checking is used in verification of many hardware circuits.This is mainly done by BDD representation which gives the stable performance.The area and power consumption in the BDD is determined by the total number of nodes present in it.Pre-computation is a powerful sequential logic optimization technique which is selectively precomputing the output logic values of the circuit one clock cycle earlier than they required.These precomputed values is used to minimize internal switching activity in the next clock cycle.These two techniques is used in designing the 8-bit magnitude comparator specially for low power gives the better performance and in reduction in area and time delay.

Keywords - BDD, Precomputation, Perfomance.

I. INTRODUCTION

In earlier days cost,area and performance are the major concerns and power is the secondary choice.The development in technology such as wireless applications,portable devices and laptops considers power dissipation as the most important factor.Digital design uses synthesis tools at the register transfer level in which the designer should use power reducing features in it.There are so many approaches to reduce the power,either by reducing voltage supply or by reducing operating voltage of the circuit.

The main goal in the Very Large Scale Integration(VLSI) design is to reduce the area of the chip and to reduce the power dissipation.The conventional magnitude comparator uses logic gates,but it takes larger area which inturn increases the wiring complexity,thus increase in power.In order to reduce area and power dissipation,BDD and pre-computation circuit is designed.These two technologies uses simpler logic that gives the better performance and reduction in chip complexity.

BDDs are the graphical representation of Boolean functions proposed by Bryant and Akers.For symbolic Boolean manipulations BDDs are the useful data structures.These have gained great popularity in discrete function representation.It is a directed acyclic graph.BDDs are used in many functions such as equivalence checking,logic synthesis,false paths and property checking.It plays significant role in minimization of a logic circuit.
Pre-computation is a powerful sequential logic optimization technique which is selectively precomputing the output logic values of the circuit one clock cycle earlier than they are required.These precomputed values is used to minimize internal switching activity in the next clock cycle,which results in reduction in area and power.

II. LITERATURE REVIEW

Average power dissipation is the important parameter in designing of general purpose and application specific integrated circuits.Optimization of power can be applied in the different levels of design.Many methods have been developed to optimize the power dissipation for CMOS combinational circuits.

The paper on "Power optimization in a 4-bit magnitude comparator circuit using BDD and Pre-computation based strategy"[1] explains about the 4-bit magnitude comparator using BDD and Pre-computation.It explains that power dissipation in BDD is lesser than the pre-computation and conventional magnitude comparator.BDD is represented by the number of nodes.If the number of nodes is minimized then the area will be reduced and in turn reduces the power dissipation.A proper polarity selection of the sub functions not only reduces the number of nodes but also switching. BDD package consists of three main components. They are BDD algorithm,Dynamic variable reordering and Garbage collection.
BDD algorithm is based on depth first traversal.BDD nodes uses complement edges for every edge,an external bit applied to indicate the function of Boolean negation.Thus it is used to encode the complement information.
The main aim of the dynamic variable reordering is to dynamically establish a better order of variable as the

computation progress.When the variable reordering starts,the operation which are currently being processed are stopped for a while.When variable reordering completes,then that initial operation continues its execution.This is based on the shifting algorithm.

It is good to have a garbage collector to remove the unwanted or unused BDD nodes.Pre-computation is a sequential logic optimization technique which is selectively precomputing the output logic values of the circuit one cycle prior than they are required.These precomputed values is used to minimize internal switching activity in the next clock cycle.
In overall this paper compares both the techniques and also the traditional magnitude comparator and found the significant improvement in the power.

The paper on ”Power optimization for low power VLSI circuits”[2] explains that in earlier days power consideration is only the secondary choice,but nowadays improvement in technology leads to look on power optimization.The power dissipation is mainly due to transistor scaling,clock frequencies and chip transistor count.There are four types of power dissipation,dynamic power dissipation,static power dissipation,short circuit power dissipation and leakage power dissipation.Optimization of the power can be done at various levels such as system level,algorithm level,architecture level,circuit level and finally technology level.System level explains about partitioning and power down.Algorithm level explains about complexity,concurrency and regularity.Architecture level explains about parallelism,pipelining,redundancy and data encoding.Circuit logic level explains about the logic styles,energy recovery and transistor sizing.Technology level explains about the threshold reduction and multi threshold devices.Optimization techniques used for low power VLSI are reduction of switched capacitance,clock gating in which clock frequency reduction is done,voltage scaling in which pipelining and hardware replication approach is used.optimization circuits used are adiabetic logic circuit which reduces the power by giving stored energy back to the supply and sleep transistor etc.A reduction of any parameters like input rise time,source leakage current,switching power and gate current etc provides lower power dissipation and provides low cost product.

The paper on “Binary decision diagrams:An improved variable ordering using graph representation of Boolean functions”[3] explains that variable ordering method to obtain the less count of nodes is Reduced Ordered Binary Decision Diagram(ROBDD).It uses graph topology to find the best variable ordering in which the Boolean input,Boolean function is converted into unidirectional graph.There are three levels of graph to obtain good variable ordering, level 1 is based on the number of paths,number of nodes and maximum number of nodes among all paths.Level 2 and level 3 is based on shortest among two variables and sum of shortest path from one variable to all the other variables.The algorithm is deterministic in which no heuristic involved in any primary parameters of the algorithm.Experimental results indicate that the reduction in the number of nodes.This algorithm is a promising alternative to existing reordering methods to reduce the number of nodes in BDD.

The paper on “Low power magnitude comparator circuit design”[4] explains about the 2-bit magnitude comparator using full adder technique and it is compared with Gate Diffusion Input(GDI) technique.It takes 2 bits of A and B i.e. A1,A0 and B1,B0 compares both and produces the result A greater than B,A less than B and A equal to B.The 2-bit magnitude comparator using full adder,GDI technique and PTL logic has been discussed.By using PTL logic,the power and area can be reduced.The PTL logic style has been used to design magnitude comparator instead of GDI technique,so as to reduce the fabrication complexity.

The paper on “Precomputation based sequential logic optimization for low power”[5] explains about the different precomputation architectures.At first synthesis of the precomputation logic has been done which compares the output for the subset of inputs,the output logic circuit can be turned off if the output can precomputed in the next clock cycle which will reduces the switching activity.It explains about the first precomputation architecture,second precomputation architecture for a finite state machine,precomputation using Shannon expansion,combinational logic precomputation presented a technique of precomputed the output value of a sequential circuit one clock cycle prior the outputs is required.This reduces the power dissipation in the next clock cycles.

CONCLUSION

The power optimization of the VLSI circuits can be done by reducing the parameters like source leakage current, input rise time, gate current etc. By reducing the number of nodes in binary decision diagrams the area and power optimization can be reduced. By using precomputation based strategy the output response of a sequential crcuit one clock cycle before the output is required.So, from all these observations the power optimization in a 8-bit magnitude comparator circuit using binary decision diagrams and precomputation based strategy can be designed. In the precomputation circuit instead of conventional magnitude comparator, BDD comparator can be used. By using these two techniques the area occupied and power consumption can be reduced.

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