FREQUENCY RESPONSE OF SERIES AND PARALLEL COMBINATION OF TWO SINGLE FEEDBACK CLASS D AMPLIFIER

[1]R. SIVARAJAN, [2]K. R. PADMAVATHY, [3]A.KASTHOORY, [4]N. SANTHA, [5]S. SUBASHRI

[1]Assistant Professor, Adhiparasakthi Engineering College, Melmaruvathur – 603319
[2,3,4,5]UG Scholar, Adhiparasakthi Engineering College, Melmaruvathur – 603319
E-mail: [1]sivarajanbeme@gmail.com, padmavathyramu93@gmail.com

Abstract- Amplifier is generally used to increase the amplitude of the signal. Consider the audio signal, if the amplitude of the audio signal is increased, then automatically loudness of the signal is increased. Class D Amplifier (CDA) consists of integrator, PWM modulator and output stage. This system can be defined as a open loop CDA system. The main factor to be considered for any amplifier circuit is the gain which is obtained by frequency response. To improve the gain of the amplifier, the various authors referred in reference designed a CDA system with closed loop with single and double feedback. Double feedback CDA has higher gain compared to single feedback CDA system. To improve the gain further, we proposed two methods – series and parallel combination of two single feedback CDA systems.

Keywords- Frequency, Parallel Combination, Amplifier, PWM Modulator, Improve the Gain, etc.

I. INTRODUCTION

One of the power handling devices is the Class D amplifier (CDA) in which its output switches over from 1 to 0 and 0 to 1. Since the power handling devices works as a binary switch, no time will wasted in between the transition of stages and no power is wasted in the zero input condition. CDA is necessary because of power efficient compared to Class A, Class B and Class AB. Ideally we know that Class AB have theoretical efficiency of 78.5% but in practical scenario with real speakers as load whose impedance from 4 to 8 ohm, the efficiency can drop as low as 50%. But in the same case, a well-designed CDA with real speakers as load will not go below 90% in terms of efficiency where in ideal case, its efficiency 100%. It passes all current through the amplifier when an ideal binary switch is ON with no voltage across it. No current will flow through amplifier when it is OFF, and the entire voltage remains across it. From the above statement it is clear that no power is wasted across the switching element which does the amplification, and it accounts for the fantastic efficiency of the CDA. But in class AB amplifier, some current will always passing through the amplifier and some voltage remains across the switching element.

A typical Class D power amplifier consists of a integrator, PWM modulator, switching circuit, and a low pass filter. An integrator is a circuit whose output signal is the time integral of its input signal. PWM modulator consists of comparator which has two inputs, message signal which is an audio signal and the triangular signal which is generated by sawtooth waveform generator. The frequency of the sawtooth waveform is usually selected, such that it satisfies the Nyquist criterion, which is 10 times the maximum frequency of interest in the input audio signal. The function of the comparator is to digitize the input audio signal by fraternization it with the chopping sawtooth waveform. The result of this fraternization will be a digital replica of the analog input signal. The low frequency constituents of the digital signal will characterize the input audio signal and the high frequency constituents of the digital signal are of no concern. Even though the output of the comparator is a digital depiction of the input audio signal, it doesn't have the power to drive the load (speaker). So, we need to add the switching circuit which provides enough current and voltage gain, essential for an amplifier. The switching circuit is generally designed around MOSFETs. To separate the low frequency components from the output of switching circuit, low pass filter is used. The output of the low pass filter will be a scaled imitation of the input audio signal. To improve the gain, Negative feedback loops are included between the low pass filter output and the comparator. The benefits of CDA are low heat dissipation, reduced size and weight and high power conversion efficiency, almost all power drawn is supplied to the load. The disadvantages of CDA are that it requires a very clean and stable power supply, and its high frequency response is dependent on the loudspeaker impedance.

One of the task done by the paper [1] is to propose a double feedback CDA amplifier and to determine the loop gain. From this paper, it is clear that loop gain is increased from single feedback CDA to double feedback CDA. The paper [2] derived the mathematical model of the second order CDA with negative feedback. Also it derives the fundamental and third order harmonics of the output signal. The paper [3] presented a comprehensive mathematical analysis of the intrinsic distortion of a BD-modulated closed-loop Class-D amplifier. It demonstrates that the unique intrinsic distortion properties of a BD-modulated design, as compared to its AD-modulated counterpart. The paper [4] presented a

3-W-per-channel CDA in 110-nm CMOS. This paper uses H bridge linearity which enables superior harmonic distortion. This paper achieves 95dB SNR and 45 dB power supply rejection.

II. OBJECTIVES

The objectives of designing class D amplifier are to provide high gain at any frequency. This paper provide how the gain of the amplifier to be increased by our proposed method.

III. EXISTING METHODOLOGY

3.1 Open Loop CDA (OLCDA)
We already had seen from the previous section that the class D amplifier section comprises of integrator and PWM modulator, which is known as open loop CDA, shown in figure 1.

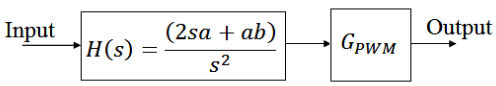

Figure 1 Open Loop CDA System

We know that, since H(s) and G_{PWM} are in series, the overall transfer function of open loop CDA is given by

$$H_{OL}(s) = \frac{(2sa + ab)G_{PWM}}{s^2}$$

3.2 Single Feedback CDA (SFCDA)
To improve the gain of the amplifier, feedback is employed in the class D amplifier in paper [1] with the feedback path of β_{fb}, which is shown in figure 2.

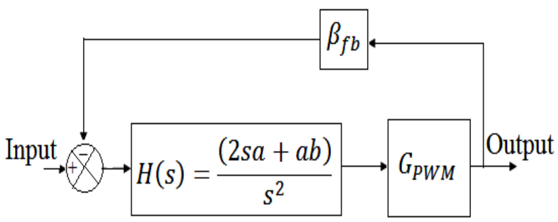

Figure 2 Single Feedback CDA systems

First H(s) and G_{PWM} are in series; hence open loop transfer function is given by

$$H_{OL}(s) = \frac{(2sa + ab)G_{PWM}}{s^2}$$

3.3 Double Feedback CDA (DFCDA)
Then feedback is employed in the open loop transfer function, then the overall transfer function becomes

$$H_{SFCDA}(s) = \frac{(2sa + ab)G_{PWM}}{s^2 + (2sa + ab)G_{PWM}\beta_{fb}}$$

To further improvement of gain the paper [1] also provides double feedback which is modeled as shown in figure 3

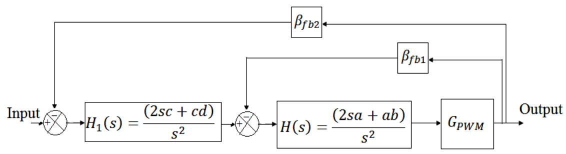

Figure 3 Double Feedback CDA System

3.4 Result as in [1]
The paper [1] shows that the gain of the double feedback CDA system improves compared to single feedback CDA system and its frequency response obtained from the paper [1] as shown in figure 4. From the graph, it is clear that the less gain is obtained at higher frequency.

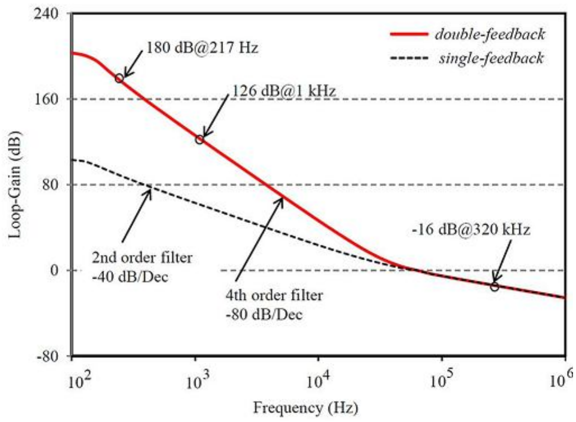

Figure 4 Frequency Responses as in [1]

IV. PROPOSED METHODOLOGY

So, to improve gain further in high frequency, we proposed two techniques by connecting two CDA amplifiers in (i) parallel and (ii) series.

4.1 Parallel SFCDA
Figure 5 shows the system in which two CDA amplifiers connected in parallel.

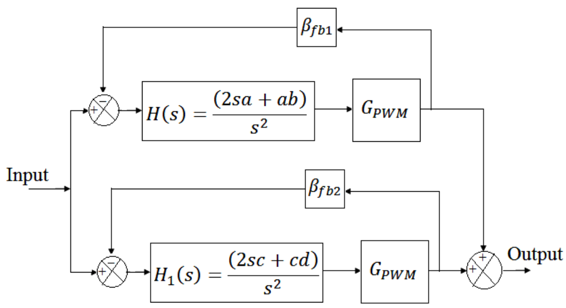

Figure 5 Two CDA amplifiers in parallel

The transfer function of two individual Single Feedback CDA connected in parallel is given as

$$H_{SFCDA1}(s) = \frac{(2sa + ab)G_{PWM}}{s^2 + (2sa + ab)G_{PWM}\beta_{fb1}}$$

$$H_{SFCDA2}(s) = \frac{(2sc + cd)G_{PWM}}{s^2 + (2sc + cd)G_{PWM}\beta_{fb2}}$$

Hence the transfer function of two Single Feedback CDA connected in parallel is given as

$$H_{SFCDA_{parallel}}(s) = H_{SFCDA1}(s) + H_{SFCDA2}(s)$$

$$H_{SFCDA_{parallel}}(s) = \frac{(2sa + ab)G_{PWM}}{s^2 + (2sa + ab)G_{PWM}\beta_{fb1}} + \frac{(2sc + cd)G_{PWM}}{s^2 + (2sc + cd)G_{PWM}\beta_{fb2}}$$

4.2 Series SFCDA

Figure 6 shows the system in which two CDA amplifiers connected in series.

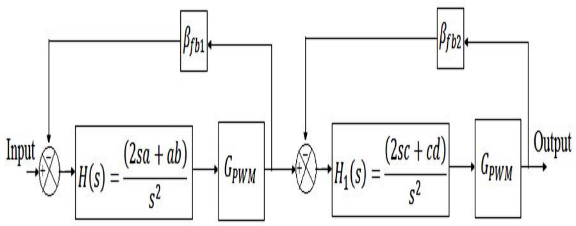

Figure 6 Two CDA amplifiers in series

The transfer function of two CDA systems connected in series is given as

$$H_{SFCDA_{series}}(s) = H_{SFCDA1}(s)H_{SFCDA2}(s)$$

$$H_{SFCDA_{series}}(s) = \frac{(2sa + ab)(2sc + cd)G_{PWM}^2}{[s^2 + (2sa + ab)G_{PWM}\beta_{fb1}][s^2 + (2sc + cd)G_{PWM}\beta_{fb2}]}$$

V. RESULTS AND DISCUSSIONS

PWM modulator is designed using comparator in which one input is message signal (sinusoidal waveform) and other input is carrier sawtooth waveform.

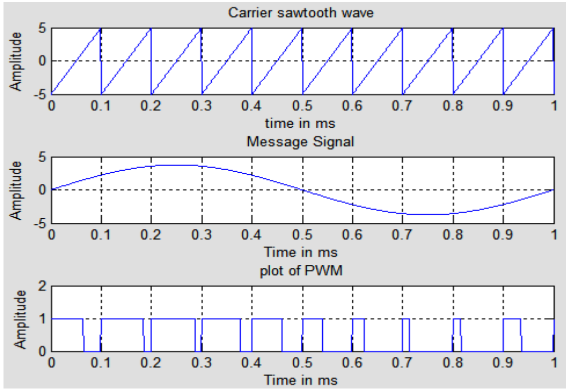

Figure 7 PWM Waveform

Figure 7 shows the input and output waveform of the PWM modulator.Figure 8 shows the frequency response of the PWM modulator.

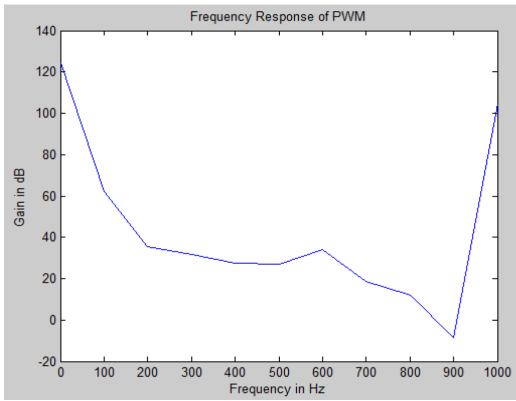

Figure 8 Frequency Response of PWM modulator

From the response graph, it is seen that the gain of the PWM modulator at 1 kHz is 188. Hence Gain in dB is equal to 105 dB so we assume G_{PWM} in entire paper as G_{PWM} = 188. The results are obtained by assuming f_c=1kHz, a=500, b=600, c=700, d=800, G_{PWM}=188, β_{fb1}= β_{fb2}=0.001.For the above assumed values, frequency response of all type of CDA system is as in table 1 and figure 9.

F (Hz)	OLCDA	SFCDA	DFCDA	Series SFCDA	Parallel SFCDA
1	283	138	64	276	152
2	255	138	36	276	152
4	228	138	9	276	152
8	200	139	-18	277	152
16	173	141	-46	281	154
32	148	148	-73	293	160
64	127	131	-101	274	151
128	110	111	-129	231	130
256	95	95	-157	198	113

512	81	81	-184	169	99
1024	67	67	-212	141	85
2048	53	53	-240	114	71
4096	39	39	-268	86	57
8192	25	25	-295	58	43
16384	12	12	-323	30	29
32768	-1	-1	-351	3	15
65536	-15	-15	-378	-24	1
131072	-29	-29	-406	-52	-12
262144	-43	-43	-434	-80	-25
524288	-57	-57	-462	-107	-39
1048576	-71	-71	-489	-135	-53

Table 1 shows Gain for various systems for different values of frequencies

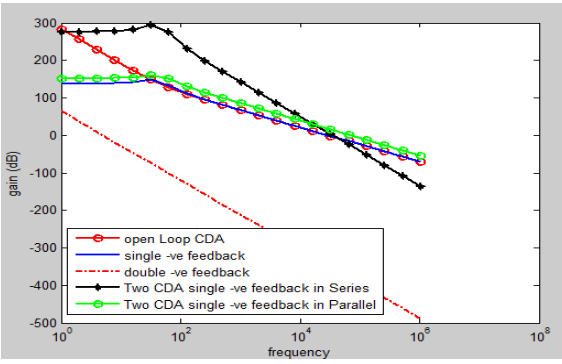

Figure 9 Comparison graph of Frequency response of all type of CDA system

From the table and graph, it is clear that series and parallel SFCDA got high gain compared to existing open loop CDA and closed loop CDA systems. Also it is clear that gain of series SFCDA is better than parallel SFCDA. But it will be true only below the frequency somewhat in between 16 and 32 kHz. Above that particular frequency, parallel SFCDA has higher gain compared to series SFCDA.

CONCLUSIONS

Thus, we conclude that series SFCDA is preferred where the application operates at low frequency and parallel SFCDA is preferred where the application operates at high frequency.

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